

**Shri Sant Gajanan Maharaj College of Engineering Shegaon**  
**Department of Electronics and Telecommunication Engineering**

**Link of Video:** [https://onlinecourses.nptel.ac.in/noc23\\_ee115/unit?unit=65&lesson=66](https://onlinecourses.nptel.ac.in/noc23_ee115/unit?unit=65&lesson=66)

**Course Title & Course Code:** Digital System Design (3ETC03)

**Class:** Second Year (2U1)

**Semester:** III

**Name of the Course Teacher:** Mr. H. B. Patil

**Title of the innovative practice:** NPTEL Video

**Objectives/Goals of the practice:**

The primary goal of this innovative teaching practice is:

1. To enhance conceptual understanding about sequential circuit, different types of flip-flops.
2. To use visual animations to illustrate how to register serial input and serial output, with the individual clock pulse, one bit of data is shifted from this SI input into the first register, and one bit of data from the last register is shifted out. So, this is the serial input/serial output type of shift register structure.

**Use of Appropriate Methods:**

To achieve the stated goals, the following methods were implemented:

1. Graphical animations are used to understand conversion of one ff to other
2. Step-by-step motion graphics depict how Tri-State Output in Registers is working
3. Students were provided with the link of NPTEL video
4. Students were informed to check the link before coming to class to enhance understanding.
5. Short quiz was conducted to do an assessment of student understanding

Significance of Results:

6. Enhances conceptual clarity and engages visual learners.

**Effective Presentation:**

1. Link was shared with all students
2. Short quiz was conducted to assess student understanding

## Photo of the activity

Lecture 31 : Sequential Circuits (Contd.)

### D to SR

Conversion Table

S-R Inputs		Outputs		D Input
S	R	Q <sub>n</sub>	Q <sub>n+1</sub>	
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	Invalid	Don't care	
1	1	Invalid	Don't care	

K-map

S	R	Q <sub>n</sub>	Q <sub>n+1</sub>
0	0	0	1
0	1	0	0
1	0	1	1
1	1	X	X

$D = S + \overline{R}Q_n$

Logic Diagram

NPTEL ONLINE CERTIFICATION COURSES

2:55 / 28:46 • D to SR

Go to Settings to activate Windows

### PO's & PSO's Mapped:

PO1, PO2, PO3, PO4, PO6, PSO1, PSO2

### Reflective Critique:

The link of NPTEL video was shared with other faculty members.

Mr. V. K. Bhangdiya suggested that content of the video more than the content of syllabus

### Evidences of success:

Increased Student Engagement :75% of students have gone through the video and actively participated in the quiz.

### Challenges faced during implementation:

It is hard to keep a track of who watched the video attentively.

**Link for peer review :** <https://forms.gle/C7ou6VUouxgyU2NDA>