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Ph : +918669638081/82
Fax : 091-7265-252346
Email.principal@ssgmce.ac.in, registrar@ssgmce.ac.in
Website- www.ssgmce.ac.in

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1	Prof. P.K.Bharne	--	Stock Market Prediction Using Artificial Neural Networks	Computer Science and Engineering	Click here
2	Prof. P.K.Bharne	--	Comparative Analysis of Recent Neuro Fuzzy Systems For Stock Market Prediction	Computer Science and Engineering	
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Ph : +918669638081/82
Fax : 091-7265-252346
Email.principal@ssgmce.ac.in, registrar@ssgmce.ac.in
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College of Engineering,Shegaon.

Stock Market Prediction Using Artificial Neural Networks

Publisher: IEEE

Pankaj K. Bharne ; Sameer S. Prabhune All Authors

Abstract: Anticipating securities exchange precisely has dependably charmed the market analysts. During the previous couple of decades different AI strategies have been connected t... **View more**

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Abstract:

Anticipating securities exchange precisely has dependably charmed the market analysts. During the previous couple of decades different AI strategies have been connected to ponder the very stochastic nature of financial exchange by catching and utilizing dull examples. Stock exercises evaluating are an intense interest for stock clients. This stock evaluating is a testing issue. Henceforth, we should a need to create application that is able to precisely foresee bearings of stock value movement. Forecasting and anticipating the patterns of market is the most critical utilizations of securities exchange. It likewise reveals the future market conduct which dependably encourages the speculators to comprehend when and what stocks can be obtained for the development of their venture. For this reasons, a considerable lot of the explores have been done as such far in the territory of investigating the financial exchange utilizing information mining.

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I. INTRODUCTION

Comparative Analysis of Recent Neuro Fuzzy Systems For Stock Market Prediction

Pankaj K. Bharne ; Sameer S. Prabhune All Authors

Abstract:
The fuzzy logic and neural networks are the two powerful techniques commonly used in various application field from their evolution. The combination of both techniques is commonly termed as Neuro-Fuzzy System (NFS). Both techniques are combined because they overcome the limitations of each other. Basically, this model is used to construct the complex model by using fuzzy logic and its capabilities are improves with a neural network. In NFS, fuzzy rules are adjusted by the input-output patterns of a neural network. This paper presents the use of this powerful NFS system in the fields of stock market application for stock price prediction. Most of the traditional approaches do not consider all kind of stock price movements. But literature proves that the NFS is a leading technique in stock market prediction. This paper initially describes the brief description of neural networks and Fuzzy logic system along with their pros and cons. Further discussing, how the advantages of both systems combined in NFS. Also, the different types and architectures of NFS are presented here. Finally, this paper studies the recent NFS dependent methods which is used for the prediction of stock market. This paper summarizes the analysis of these techniques based on the technique used, the dataset used, their advantages and some research gap of all these techniques.

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Novel Technique For Detection Of Power Quality Disturbance

Arati S. Ambhore
P. G. Student,
Dept. of Electrical Engineering,
SSGM College of Engineering,
Shegaon (M.S.), 444203, India
aratiambhore95@gmail.com

Dr. S. R. Paraskar
Professor,
Dept. of Electrical Engineering,
SSGM College of Engineering,
Shegaon (M.S.), 444203, India
srparaskar@gmail.com

G. N. Bonde
Assistant Professor,
Dept. of Electrical Engineering,
SSGM College Of Engineering,
Shegaon (M.S.), 444203, India
ganeshbonde2009@gmail.com

***Abstract*— This paper presents the detection of power quality (PQ) events using mathematical morphology and classification of the events using statistical parameter such as standard deviation. The mathematical morphology is used to detect the events. By using mathematical morphology the feature is extracted that is morphological gradient. The morphological gradient can be determined from the erosion and dilation of the given test signal. At start of the event the morphological gradient gives the pulse as well at the end of the event pulse is obtained. So the threshold value is set based on to the normal voltage signal without disturbance. If the morphological gradient exceeds the threshold value the flag goes high and it indicates the initiation of events similarly at end of the events the flag goes high. The statistical parameter such as standard deviation (STD) is used for the classification of the events such as voltage sag, voltage swell and interruption. The STD is determined for half cycle from the initiation of the events again the threshold value is set for the classification. The five samples of the voltage sag, swell and interruption events are recorded using the trailer made experimentation in the laboratory. The methodology is tested over it. The method is very easy as well as simple to implement and faster. It works with the experimental data consisting a lot of noise; this is the strength of the algorithm.**

Keywords*— *Power Quality disturbances, Mathematical Morphology, Morphological gradient, Standard Deviation

I. INTRODUCTION

In the early years, power quality disturbances became a growing problem for electric utilities and customers [12]. In general, anything that causes a difference in current or voltage with respect to the ideal sinusoid can be considered a disturbance in power quality [13]. In recent decades significant energy and economic losses have been reported due to increasing disorders, which increasingly concern towards researchers [14]. More and more disturbances in the electrical network are caused by the increasing use of non-linear loads. Demanding electronic devices can be damaged even if the disturbance is sometimes slight. For this reason, power quality (PQ) has become a problem for public services and the manufacturing industry [4]. This is why it is important to correctly detect power quality disturbances.

To identify and classify power quality events, numerous algorithms have been proposed that give satisfactory results. The analysis of current and voltage data sets with frequency based approaches is a common method for measuring PQ noise. This classical method of PQ analysis is based on the Fourier transform (FT), i.e. the fast Fourier transform, the discrete Fourier transform and so on. Although these methods are easy to implement, they have serious drawbacks. The length of the fixed window does not detect the transients. As a result, an adaptive data window is being used by some method to extract transients [2].

The wavelet transformation (WT) is a powerful transient extraction tool commonly used to detect and analyze PQ events [3]. However, the performance of WT-based methods largely depends on the correctly selected main wavelets. Furthermore, they require a variety of calculations that can affect their real-time performance [2]. Consideration of the above problems with respect to FT and WT based methods; this document combines a mathematical morphology (MM) based on information on the form of the signal [2]. The proposed document implements a new method by calculating the statistical parameter and the threshold method. At the start of the event the standard deviation detection indicator (STD) is calculated. Table I. shows the STD range.

The other part of the article is given as follows. Section II gives the information about PQ disturbances. Section III shows the mathematical morphology and the mathematical morphology based algorithm, these section gives more information about morphological gradient and the threshold value. Section IV Shows the experimental setup. The results and discussion are reported in Section V. Finally, some conclusions is made.

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[10] Q. H. Wu, Z. Lu, and T. Y. Ji, "Protective Relaying of Power Systems Using Mathematical Morphology," 1st ed. Springer Publishing Company, Incorporated, 2009.

[11] Lu Z, Smith J S, Wu Q H. "Morphological lifting scheme for current transformer saturation detection and compensation," in IEEE Transactions on Circuits and Systems I: Regular Papers (Volume: 55 , Issue: 10 , Nov. 2008).

[12] Y. Zhang, T. Ji, M. Li, and Q. Wu, "Detection and classification of low frequency power disturbances using a morphological max-lifting scheme," in 2013 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC).

[13] Ozal YILDIRIM "An Online Electric Power Quality Disturbance Detection System," In 51st International Universities Power Engineering Conference UPEC2016, At Portugal.

[14] M.H.J.BOLLEN, " Signal Processing of power Quality Disturbances."

[15] M.H.J.BOLLEN, "Understanding power Quality Problems Voltage Sags and Interruptions". New York IEEE Press, 1999, Vol. I.

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Locating the Fault on Transmission Line using Wavelet Based ANN Approach

1st Minal Gedam
Electrical Engineering Department
S.S.G.M College of Engineering
Shegaon (MS) India 444203
minalgedam0307@gmail.com

2nd Prof. P. R. Bharambe
Electrical Engineering Department
S.S.G.M. College of Engineering
Shegaon (MS) India, 444203
prbharambe@ssgmce.ac.in

***Abstract* — Protection of power system from various faults on transmission line is one of the major issues. Finding the exact location of the fault on transmission line and categorizing the type of fault provides an efficient solution. Finding exact location of fault provides one of the best capabilities to improve efficiency of protecting relays in power system. In this paper a new approach is developed using wavelet transform and artificial neural network for determining the location of fault on transmission line. This technique bears a new developed algorithm which can locate eleven types of fault over 100% length of transmission line. The location of fault is calculated by extracting the features of current or voltage signal using wavelet transform succeeded by use of neural network. The algorithm developed has a very high degree of accuracy, reliability and robustness resulting improved results compared to existing techniques.**

Keywords* — *Fault location, Artificial Neural Network, Transmission line, Wavelet Transform.

I. INTRODUCTION

With wide need of uninterrupted power supply, presently a day's power supply has turned into the business item. To stay in rivalry; the continuous power supply must be given to the consumers. Power supply system comprises of generation transmission and distribution area. Occurrence of fault on any of these may prompt interference of supply or uninterrupted power supply to consumers. The fundamental capacity of the electrical transmission and distribution system is to transfer electrical energy from the generating unit to the utility and finally to the consumers [1]. For the most part, whenever fault do occur on the transmission line, determining/distinguishing the fault and clearing it is very much essential as it may damage the transmission line and power system equipment too. For the same, the vigorous demand for reliable technique have emerged development of easy and fast response new techniques of fault detection. In order to protect transmission line, the well-known techniques used so far is distance protection, where impedance between relay and fault point is calculated at fundamental frequency from the voltage and current signals and the calculated impedance indicates the fault. Nowadays, adaption of digital relaying, Fuzzy logic, signal processing, ANN approach etc. has improved the overall performance in protection. The application of wavelet transform has improved the capability of identifying the transient signals in the power system [2]. The neural-network based methodologies have been gaining an attention in recognizing the type and location of fault yet it requires a lot of preparing exertion in good execution of method, particularly during variations in working conditions such as, varying fault resistance, system loading, and inception instance of fault and so on. Wavelet based system alone when used to recognize the fault has cumbersome behavior in computing. Similarly, other detection techniques are either complex or time consuming. Be that as it may, the fuzzy logic based method is comparatively faster but limited to detect only nature of fault i.e. LG or LLG and inoperative exactly the phases involve in fault occurrence [3]. On the other hand, in recent years, use of fault generated travelling wave methodology is taken into consideration for identifying the fault location and protection of power transmission line. In this method, a fault distance on transmission line is determined by measuring the time difference (at sending end) in between the incident wave and reflected wave from fault location but due to limitation in bandwidth of CT and VT such method fails to avail satisfactory results [2] [4] [5]. Several methods of fault location using low frequency do exist till date but are less effective since most of the transients condition that occurs due to high frequency signals are neglected/missed thereby affecting the exactness in fault identification. Thus, the method in co-ordination with wavelet transform the artificial neural network along with neural network can be useful for locating the faults on power cables [6].

II. DEVELOPMENT OF MODEL

The proposed method for fault identification on transmission line is extensively tested on 132 kV, 50 Hz, 43 km length of transmission line. Fig 1 indicates the simplified model of power system, where transmission line of 43 km is considered to be connected between two sources. Operation of relay is in ordinance with fault on transmission line. The work represented in this paper is mainly depends of identification of total number of 11 types of faults on transmission line.

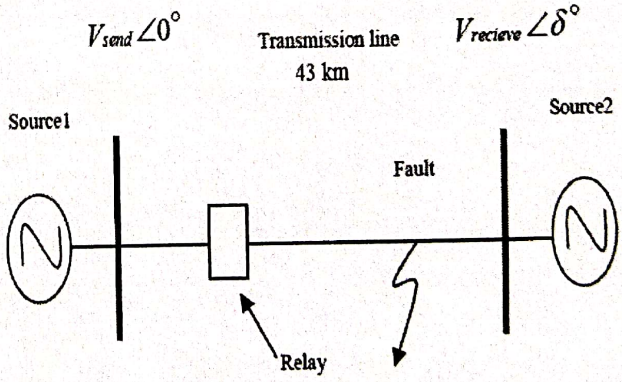

Fig.1: Power System Model

at a distance of 34 km for 50kV, 375kA of voltage and current respectively.

VI. Conclusion

The wavelet transform based ANN approach for identifying the exact fault location have been developed which offers several advantages in terms of good response time and frequency localization characteristics over other conventional methods of fault identification on transmission line. The wavelet components can be used as a feature in locating the fault later an ANN approach developed with trained models can exactly classify and locate the fault. The combination of WT, ANN, LM algorithm surely adopts the fault condition and accordingly exact fault location can be observed with series of test conducted during verification of results. It adds robustness in fault identification and also gives high accuracy in dealing with variety of faults on the system.

References

[1] Xiangjun Zeng and Yuanyun Wang, " Faults detection for Power System", IAS Annual Meeting, IEEE industry application society New Orleans LA, pp. 71 – 118.

[2] Jamal Moshtagh and R. K. Aggarwal, " A new approach to underground fault location in a three-phase underground distribution system using cobined neural network & wavelet analysis", IEEE CCECE/CCGEI Ottawa, May 2006.

[3] Alessandro Ferrero and Siliva Saniovanni, " A Fuzzy-set approach to fault type identification in Digital Relaying," IEEE Trans. on Power Delivery. Vol. 10. Jan 1995. pp. 169-175.

[4] A. Abdollahi and S. Seyedtabaii, " Transmission Line Fault Location Estimation By Fourier Transform using ANN" 4th International Power Engineering and optimization conference (PEOCO2010), Shah Alam, Malaysia, 23-24 June 2010.

[5] Seema Singh, Mamatha K.R. and S. Thejaswini, " Intelliegent fault identification Systems for transmission Lines using Artificial Neural Network, IOSR journal of computer engineering vol. 16, issue 1 Jan 2014, pp. 23-31

[6] Anamika Jain, " Artificial Neural Network based fault distance locator for double circuit transmission Line," Hindwi Publishing corporation Advances in Artificial Intelligence, 2013, Article ID 271865. 12 Pages

[7] Springer-verlag, " Daubechies Ten Lectures on Wavelet" YZ

[8] Alessandro ferrero and Silvia Sangiovanni, " A Fuzzy-Set approach to fault type identification in Digital Relaying, IEEE transaction on Power Delivery, vol 10, pp. 169-175, Jan 1995.

[9] P.S Bhowmik, P. Purkait, K.Bhattachary," A novel wavelet transform aided Neural Network based transmission line fault analysis method," electrical powr and energy systems 31(2009) pp. 213-219.

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3.3.2 Number of books and chapters in edited volumes/books published and papers published in national/ international conference proceedings per teacher during last five year

Sl. No.	Name of the teacher	Title of the book/chapters published	Title of the paper	Title of the proceedings of the conference	Name of the conference	National / International	Year of publication	ISBN number of the proceeding	Affiliating Institute at the time of publication	Name of the publisher
1	L. SAMAL	NA	Study and analysis of Low Power Dynamic Comparatorfor IOTApplication	Journal of IEEE Bombay Section Signature Conference – IBSSC-2019	IEEE Bombay Section Signature Conference – IBSSC-2019	International	2019	978-1-5386-7401-7	Shri Sant Gajanan Maharaj College of Engg., Shegaon	IEEE
2	L. SAMAL	NA	Application Specific Instruction Set Processor Design for Embedded Application Using The CoWare Tool	Journal ofInternational Conference on Innovative Trends and Advances in Engineering and Technology (ICITAET)	International Conference on Innovative Trends and Advances in Engineering and Technology (ICITAET)	International	2019	978-1-7281-1901-4	Shri Sant Gajanan Maharaj College of Engg., Shegaon	IEEE
3	Dr. M.N. Tibdewal	NA	Analysis of Electroencephalogram for Cognitive Effects of Human Being Before and After Meditation	Journal of IEEE Sponsored International Conference on "Industry 4.0 Technology 2020	IEEE Sponsored International Conference on "Industry 4.0 Technology 2020	International	2020	978-1-7281-5003-1	Shri Sant Gajanan Maharaj College of Engg., Shegaon	IEEE

Dr R.S.Dhekekar/ Dr D.P.Tulaskar/Mrs. K.M.Thanvi
co-ordinators

S.S.G.M.C. SHEGAON-444203 (M.S.) INDIA
Department of Electronics & Telecomm. Engg.

Dr.M.N.Tibdewal
HOD, EXTC

Study and analysis of Low Power Dynamic Comparator for IOT Application

Lopamudra Samal
Department of ECE
SSGMCE, Shegaon, India
lopamudrasamals@gmail.com

Dr P. Karuppanan
Department of ECE
MNIT Allahabad, India
pkaru@mnnit.ac.in

Prem Kumar
Department of ECE
MNIT Allahabad, India
prem.8293@gmail.com

Sauvagya Ranjan Sahoo
Department of ECE
NIT Rourkela, India
sauvagya.nitrl @gmail.com

Abstract— **The Internet of Things (IoT) applies the sensors and MCUs on various machines, devices and equipment, and connect them through internet. This brief presents the design of a low power dynamic comparator circuit which is compatible with wide range of applications (i.e., internet of things (IoT) sensors and integrated analog to digital convertor).In this paper different types of comparator-Conventional dynamic comparator, double tail dynamic comparator and dynamic comparator with enhanced latch regeneration speed have been analyzed. Dynamic comparator with enhanced latch regeneration speed is better than previous two conventional dynamic comparator in terms of power and speed.**

Keywords: Internet of Things (IoT) ,VLSI Design, Dynamic comparator, power, speed

I. INTRODUCTION

The Internet of Things (IoT) will transform our world. Connecting all of the "things" that touch our everyday lives through sensors and cloud computing promises to unlock the door to the next industrial revolution. IoT can seem like "magic". It attracts large attention which is connecting and controlling machines, devices and equipment through network. By using the IoT, a lot of sensors are required in the system for collecting the data or information such as humidity, temperature, magnetic field strength, strain and motion, etc. from past few years, there has been a rapid growth in need of wireless sensor nodes for the internet of things (IoT) applications. This growth has led to evolutional milestones in IoT applications such as home automation, healthcare and environmental/manufacture monitoring. However, these sensing nodes are not installed under normal conditions and suffer from unpredictable dynamics. Therefore, they are required to achieve extremely low-power consumption. As they are supplied by either a battery or an energy harvesting module that requires low-power and high-efficiency power management integrated circuits [1].

In today's world, battery operated devices is increasing, a major importance is given in the direction of low power approaches for high speed applications. With the rapid growth of microchip technology engineering typically portable electronics systems, which is wireless communication devices, battery-powered medical devices etc. In all these application battery life is one of the most important factors. So need of low power and low voltages is very essential. IC's cost can also reducing by using thicker oxide layer or higher supply voltages Normally, In the IC's where analog to digital convertor or digital to analog convertor plays an important role, low power and low voltage comparator is very essential and necessary thing. Comparator is the important part of ADC's and also consumes large power in device. It is essential or primary concern to achieve low power and high speed comparator. Hence, to enhance the performance of comparator, Kick back noise is to be reduces. It is generated due to the back flow of the output signal to the input. The feedback mechanism responsible for back flow which include both positive and negative feedback [2-3][9].

In recent article[4],comparator circuit is enhanced by including additional circuitry and uses 0.8 V supply voltage and consume power about 15.54 µW. Double-tail dynamic comparator structure in contains two tail transistor which makes its operation faster. Similarly in article [5], double tail dynamic comparators designed. This comparator contains two tails which give enough current for faster decision making. In supply boosted comparator [6], two differential amplifiers have been used. One differential amplifier has been used only for boosting technique but other differential amplifier has been used for regular comparator circuit. Resolution and gain of this comparator has improved with respect to previous one. Latch comparator offset is analyzed [2] in terms of its load capacitor mismatch. As offset is a very critical parameter in comparator design. If mismatch load is used then offset voltage of comparator is very high. Supply boosting technique [7] is also very common choice in comparator design. It is more suitable for low clock and low power comparator circuit. In this comparator charge pump circuit is used. This charge pump circuits boosted the clock during comparison phase. Due to this comparator circuits become faster than previous conventional dynamic and double tail dynamic comparator.

In this paper different types of comparator-Conventional dynamic comparator, double tail dynamic comparator and dynamic comparator have been studied and analyzed with enhanced latch regeneration speed. The paper is organized as follows: In section II clock based conventional dynamic comparator designs have been explained. In section III proposed comparator is explained. In section IV simulation results and discussion have been done. Finally, the conclusion is given in section V.

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II. CLOCKED BASED DYNAMIC COMPARATOR

In this Section, different procedure of the conventional and double tail dynamic comparators have been discussed.

A. Clocked based conventional dynamic comparator

This section briefly describe the delay and power consumption of different dynamic comparators.

In Fig. 2.1, the circuit design of conventional dynamic comparator is revealed. This comparator static power consumption is zero and If clk = 0 then tail transistor M_{tail} is "off". Transistors (M_7–M_8) is reset by tamparerly switched, Output voltages (O_{utn}, O_{utp}) to V_{DD}. Likewise, when clk = V_{DD},M_{tail} is "on"and transistors (M_7, M_8) are "off". In this condition O_{utp} and O_{utn} , started discharging by dissimilar discharging rates, corresponds to the input voltages (INN and INP). Let, V_{INN}< V_{INP}; then O_{utn} discharges lesser than O_{utp}, hence O_{utp}drops down to V_{DD}–|V_{thp}| earlier than O_{utn} . As a result, transistor M_5 (PMOS) will turn "on"that leads the latch regeneration due to end-to-end inverters (M_3, M_5 and M_4,M_6). Also, when for V_{INN}>V_{INP}; circuit operation is vice versa.

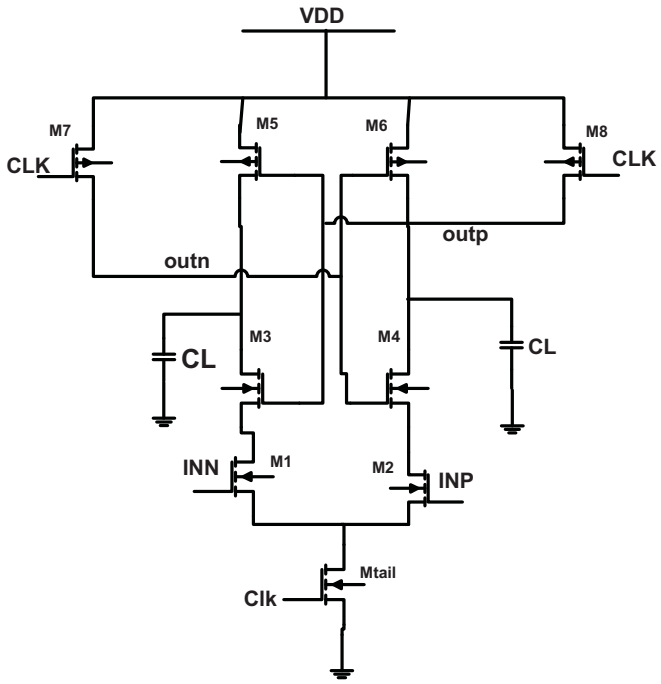

Fig 2.1Single tail dynamic comparator

The conventional dynamic comparator have two type of delay that are discharge delay (t_0) and latching delay(t_{latch}).The delay $t_0$occures owing to the capacitive discharge of the load capacitance (C_L) till the time required to transistor (M_5/M_6) turns "on". For, I_{NP}> I_{NN} the drain current (I_2) of transistor M_2getsdischarged more rapidly of O_{utp} node than O_{utn} node. The O_{utn} node is driven by M_1havinglesserdrain current. Subsequently, the t_0 is drived from:

$$t_o = \frac{C_L\ |V_{thp}\ |}{I_2} \qquad (2.1)$$

Where, t_o is the delay due to all transistor except latch, $C_L$is the load capacitance, V_{thp} is threshold voltage of PMOS transistor andI_2 is Current which is contributing to tail current.

The latching delay (t_{latch}) is the delay is due to cross-coupled inverters in the circuit and given by[8].

$$t_{latch} = \frac{C_L}{gm_{eff}} * \ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) \qquad (2.2)$$

$$t_{delay} = t_0 + t_{latch} \qquad (2.3)$$

Where t_{delay} is total delay,$t_o$is the delay due to all transistor except latch,t_{latch}isdelay due to latch, C_L is load capacitance, gm_{eff} is Effective trans-conductance, $\Delta V_{out}$is Output voltage difference. The$\Delta V_0$is measured output voltage diffrence at the dropping output.Hence,load capacitance (C_L) is directly proportional, input difference voltage (V_{in}) is indirectly proportional to total delay (t_{delay}) of comparator. Therefore, the decreased value of V_{cm}, increases the delay (t_0)due to slighter bias current (I_{tail}) hence fourth, the increased value of initial voltage difference (V_0) is obtained that decreasing t_{latch}.

For fast speed and switching operation V_{cm} requires only 70% V_{in} [8]. Also, due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time because transistors M_3 and M_4 initially contributed for positive feedback until transistors M_5 or M_6get starts. If the supply voltage is low, then vey small amount of gate source voltage (transconductance) is produced which create larger latch delay time. To obtained enhanced Gm/I ratio and long intergrted interval, lower tail current is desired to retain the differential couple in weak inversion[9-10] contrarly, for the fast generation requires a large tail current. Moreover, M_{tail} drives normally in triode region hence tail current is depends on V_{cm} and it is not suitable for regeneration. Another disadvantage of such circuit is that tail transistor (M_{tail}) have only one current path for latch and differential amplifier.

The power of the comparator is given by

$$P_{total}=P_{static} + P_{dynamic} \qquad (2.4)$$

$$P_{static} = I_{leakage} * V_{dd} \qquad (2.5)$$

Where $I_{leakage}$ is leakage current of transistor and V_{dd}supply voltage

$$P_{dynamic}= C_L * V_{dd}^2 * f \qquad (2.6)$$

Where $C_L$load capacitance, and f is the frequency of pulse

B. Clocked based double-tail dynamic comparator

In Fig. 2.2 a double-tail comparator is shown .This comparator require very low supply voltage compared to the older conventional dynamic comparator due to less stacking. Advantage of double tail is to produce huge current during latching and immediate latching, also it does not depends on V_{cm} and for low offset,a very less current at the input stage [4].When clk = zero, transistor M_{tail1}/M_{tail2} are "off"hence M_3 and M_4begins to charge node fp, fn to V_{DD} and transistor M_{R1} M_{R1} to ground. On the other hand when clk = V_{DD} both tail transitors (M_{tail1}/M_{tail2}) get "on" hence M_3 and M_4 turns "off" which leads to discharge the voltage at node fp,fn at the rate of IM_{tail1}/Cfn (p) hence intermediate differential voltage $V_{fn(p)}$ is

established which offer protection among input/output, so ,reduces the noise [5].

It can be easily seen in figure, that in evaluation phase O_{utp}, O_{utn} both node discharge and accordingly, phase gets started. So, any one phase O_{utn} or O_{utp} energies to high and alternative remain in same stage.

The time delay is analyzed by following equations:

$$t_{delay} = t_0 + t_{latch} \quad (2.7)$$

$$t_{latch} = \frac{C_L}{gm_{eff}} * \ln\left(\frac{V_{DD/2}}{\Delta V_O}\right) \quad (2.8)$$

$$t_o = \frac{C_L \, |V_{thn}|}{I_2} \quad (2.9)$$

Where t_{delay} is the total delay,t_o is the delay due to all transistor except latch, $t_{latch}$is thedelay due to latch, C_L *is the load* capacitance, gm_{eff} is the effective transconductance, $t_o$is the delay due to all transistor except latch and I_2 is the current which is contributing to tail current.

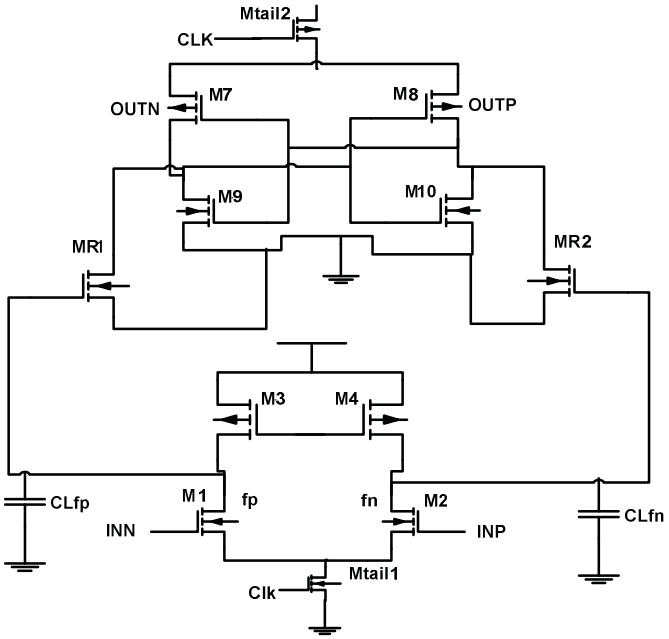

Fig. 2.2 Dynamic Comparator (Double tail)

C. Double-tail dynamic comparator with enhanced latch regeneration speed

Transistor M_{R2}, M_{R1} to ground. On the other hand when clk = V_{DD} both tail transitors (M_{tail1}/M_{tail2}) get "on" hence M_3 and M_4 turns "off" which leads to discharge the voltage at node fp,fn at the rate of IM_{tail1}/Cfn (p) hence intermediate differential voltage $V_{fn(p)}$ is established which offer protection among input/output, so, reduces the noise [5].

Fig.2.3, the modified circuit diagram of comparator is shown. When clk = zero, transistor M_{tail1}, M_{tail2} are "off" hence M_3 and M_4 begins to charge node fp, fn to V_{DD} and control transistor (M_{c1}, M_{c2}) turn "off". When clk = V_{DD}, then each tail transistor M_{tail1}, M_{tail2} turns "on", and so transistors M_3, M_4 flip "off". But still, transistors M_{c1}, M_{c2}areat "off" condition due to node fn , fp at V_{DD}. Also, voltage at fn, fp begin to drop with dissimilar rates in keeping with the input voltages. Let us anticipate a case while V_{INN}< V_{INP}, therefore fp decreases lesser than fn. When node fn remains decreasing, than respective PMOS transistor M_{c1}flip to "on", and simultaneously fp node reaches to V_{DD}. So every other M_{c2} stays "off", permitting fn to be absolutely discharged. The transconductance characteristics of comparators is mentioned in [6]. It is worth notices that static power consumption is observed due to transistor M_{c1} is activate. To conquer this problem, modified circuitry have been suggested as shown Fig.2.3, the switches of NMOS are added with Msw1 and Msw2.

The nodes of fn and fp were excited by VDD while reset operation, and fn, fp begins to fall with exclusive discharging rates so, comparator identifies quicker discharging node. The operation of the latch is emulated by control transistor switches.

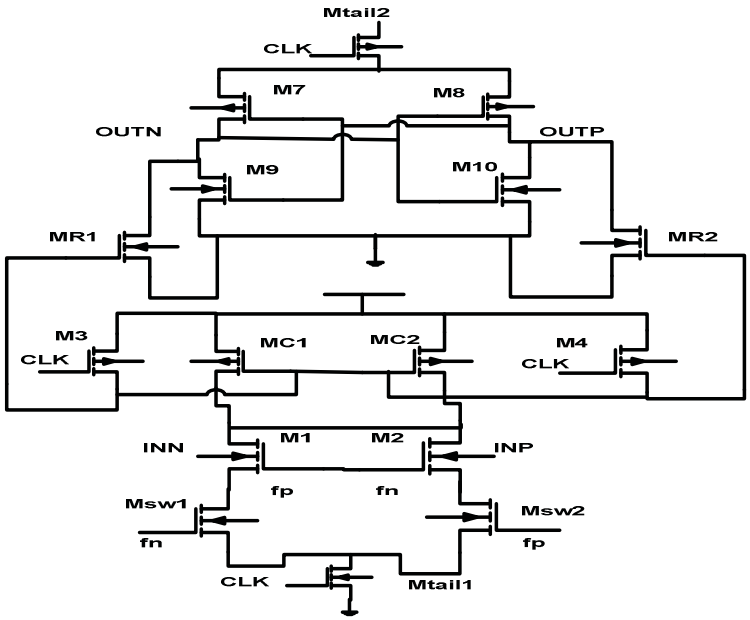

Fig 2.3 Double tail dynamic comparator with Enhanced latch regeneration speed

The Delay is analyzed by by following equations:

$$t_{delay} = t_0 + t_{latch} \quad (2.10)$$

$$t_{latch} = \frac{C_L}{gm_{eff}+gm_{r1,2}} * \ln\left(\frac{V_{DD/2}}{\Delta V_0}\right) \quad (2.11)$$

$$t_o = 2 * \frac{V_{thn} \times C_{L\,out}}{I_{tail\,2}} \quad (2.12)$$

Where $t_{delay}$is total delay,t_o is the delay due to all transistor except latch, $t_{latch}$is thedelay due to latch,$C_L$is the load capacitance,gm_{eff}- Effective transconductance, $gm_{r1,2}$ is the latch transconductance, $V_{thn}$is NMOS threshold voltage, $t_o$is the delay due to all transistor except latch and I_2 is the current which is contributing to tail current

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III. Proposed Comparator

A technique is suggested for moderates the power consumption effectively of all the transistor. The sub-threshold current can be reduced considerably by lessening the V_{DS}. The V_{DS} can be decreased by increasing source terminal voltage hence, additional transistors labeled PMOS have been used to enhance the source terminal voltage of MOSFET. As the additional PMOS transistor is at cutoff position, it produces leakage currents, consequently source voltage increases and due to this V_{DS} decreases. In Fig. 2.4, four extra PMOS transistor have been used and due to this, power of the circuit decreases up to some extent. When clk = zero, transistor M_{tail1}, M_{tail2} are "off", hence M_3 and M_4 begins to charge node fp, fn to V_{DD} and control transistor (M_{c1}, M_{c2}) turn "off". When clk = V_{DD}, then each tail transistor M_{tail1}, M_{tail2} turns "on", and so transistors M_3, M_4 flip "off". But still, transistors M_{c1}, M_{c2} are at "off" condition due to node fn , fp at V_{DD}. Also, voltage at fn, fp begin to drop with dissimilar rates in keeping with the input voltages. Let us anticipate a case while $V_{INN} < V_{INP}$, therefore fp decreases lesser than fn. When node fn remains decreasing, than respective PMOS transistor M_{c1} flip to "on", and simultaneously fp node reaches to V_{DD}. So every other M_{c2} stays "off", permitting fn to be absolutely discharged.

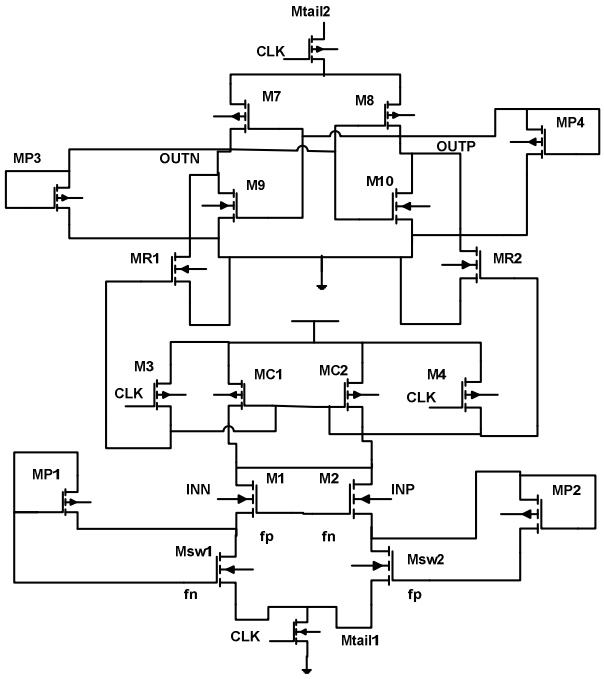

Fig 3.4 Proposed Comparator circuit

IV. Simulation Results and Discussion

For simulation purpose the cadence virtuoso gpdk 180nm technology have been used. Firstly the circuit is design, analyze of delay and power of each comparator one by one.

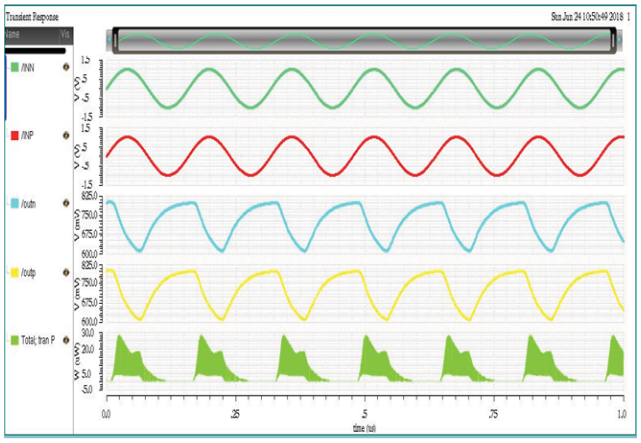

Fig.3.1 Simulation of Conventional Dynamic comparator

Conventional dynamic comparator circuit simulation is presented in Fig. 3.1,The sinusoidal input of 702.5mv and 607.5 mv to differential input have been given.Here,1pF capacitor is used at output node. Here both output are analyzed in terms of their respective input signal.Here,it can see from graph that how both output charges and discharges according to supplied input. Transient power is also analyzed in this circuit, So that it can get brief analysis of conventional dynamic comparator circuit.

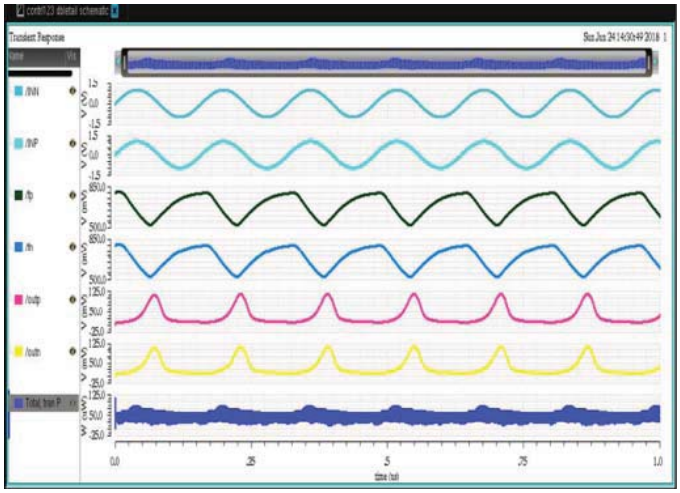

Fig.3.2 Double tail Dynamic comparator

Double tail dynamic comparator circuit simulation is presented in Fig. 3.2.The sinusoidal input of 702.5 mv and 607.5 mv to differential input have been given.Here,1pF capacitor is used at output node. Here both output are analyzed in terms of their respective input signal. Here, it can see from graph that how both output charges and discharges according to supplied input. Output plot is more accurate than conventional dynamic comparator. This due to two tail present in this circuit. Extra tail provides enough current for faster decision making in comparator circuit. The transient power is also analyzed in this circuit, So that it can get brief analysis of conventional dynamic comparator circuit.

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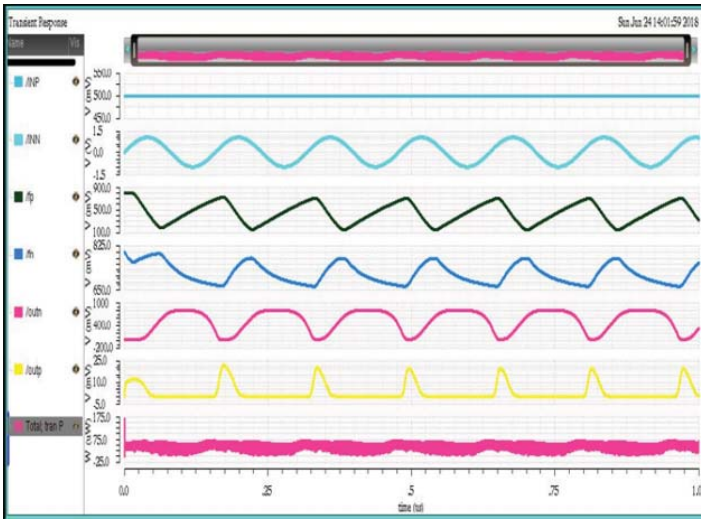

Fig. 3.3 Double tail comparator when one of it's input is d.c voltage

Double tail dynamic comparator circuit simulation is presented in Fig.3.3 for d.c input. The sinusoidal input of 702.5mv and 500mv as a reference voltage to differential input have been given.Here,1pF capacitor is used at output node. The supplied constant voltage source to one of its input, so that it can get better understanding of output response. Here both outputs are analyzed in terms of their respective input signal. Here,it can see from graph that how both output charges and discharges according to supplied input. Transient power is also analyzed in this circuit, So that it can get brief analysis of conventional dynamic comparator circuit.

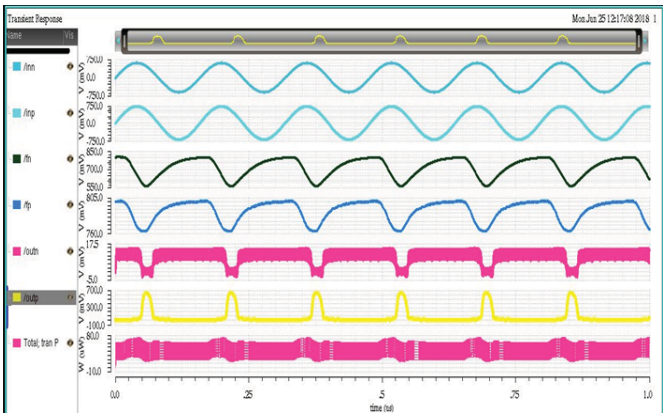

Fig.3.4 Double tail comparator with enhanced latch regeneration speed

Double tail dynamic comparator with enhanced latch regeneration speed circuit simulation is presented in Fig 3.4,The supplied sinusoidal input of 702.5mv and 607.5 mv to differential input.Here,1pF capacitor is used at output node. Here both outputs are analyzed in terms of their respective input signal. In this comparator two latches have been used, due to this decision making operation becomes faster .As it can see from the corresponding output graph. Here it can see from graph that how both output charges and discharges according to supplied input. Output plot is more accurate than double tail dynamic comparator. This due to two tail present as well as two latches is present in this circuit. Extra latch provides enough current for faster decision making in comparator circuit. Transient power is also analyzed in this circuit, So that it can get brief analysis of dynamic comparator circuit with enhanced latch regeneration speed.

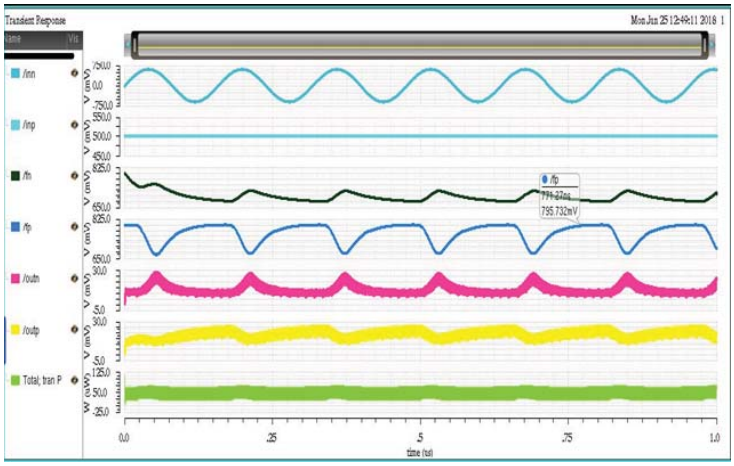

Fig 3.5 Dynamic comparator with Enhanced latch regeneration speed when one of its input is d.c voltage

Dynamic comparator with enhanced latch regeneration speed circuit simulation is presented in Fig.3.5 for d.c input, The sinusoidal input of 702.5mv and 500mv constant d.c voltage to differential input is provided.Here,1pf capacitor at output node is used and both output are analyzed in terms of their respective input signal. The constant voltage source is supplied to its any input, so that gets better understanding of output response .In this comparator two latch has been used, due to this decision making operation becomes faster .Here, it can see from graph that both output charges and discharges according to supplied input. Output plot is more accurate than double tail dynamic comparator. This due to two tail present as well as two latches is present in this circuit. Extra latch provides enough current for faster decision making in comparator circuit. Transient power is also analyzed in this circuit, So that it can get brief analysis of dynamic comparator circuit with enhanced latch regeneration speed.

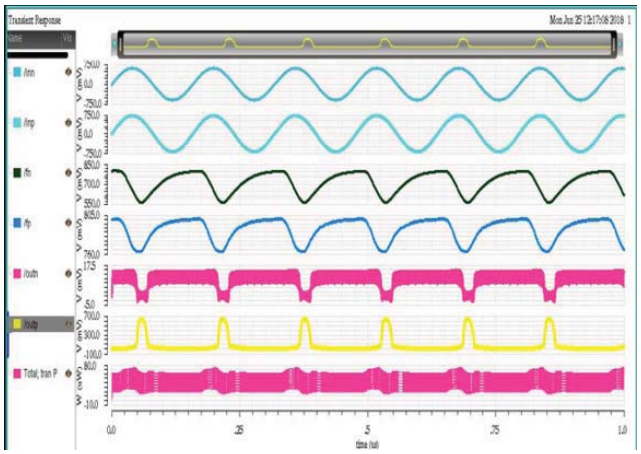

Fig. 3.6 Proposed Comparator when sinusoidal input is applied

Proposed dynamic comparator circuit simulation is presented in Fig 3.6. The feed sinusoidal input of 702.5mv and 607.5 mv to differential input. Here, 1pF capacitor is used at output node In this Simulation Output is same as Enhanced latch regeneration speed comparator.But this proposed circuit is power efficient.Here both output are analysed in terms of their respective input signal.In this comparator two latch has been used,,due to this decision making operation becomes faster . In graph it is clearly seen from the corresponding output.Here,it can seen from graph that how both output charges and discharges according to supplied input.Output plot is more

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accurate than double tail dynamic comparator.This due to two tail present as well as two latches is present in this circuit.Extra latch provides enough current for faster decision making in comparator circuit.Tratnsient power is also analysed in this circuit,So that it can get brief analysis of dynamic comparator circuit with enhanced latch regeneration speed.

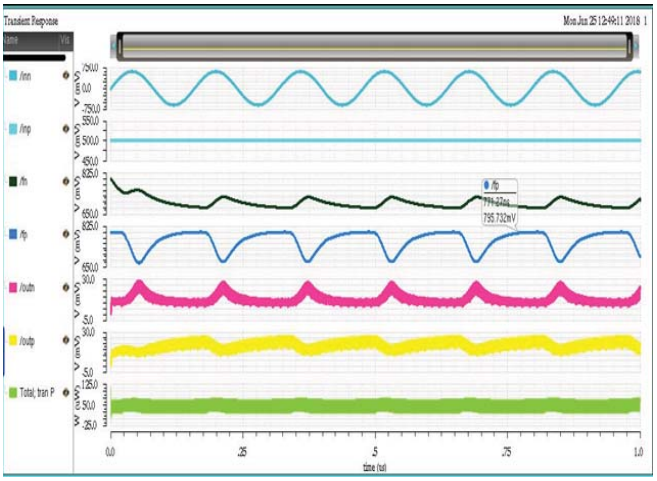

Fig3.7 Proposed dynamic comparator circuit when one of its input is d.c voltage

Proposed dynamic comparator circuit simulation is presented in Fig.3.7 for d.c input. The assumed sinusoidal input of 702.5mv and 500 mv constant d.c voltage to differential input.Here,1pF capacitor is used at output node. Here both output are analyzed in terms of their respective input signal. node In this Simulation Output is same as Enhanced latch regeneration speed comparator.But this proposed circuit is power efficient.The supplied voltage source is constant to one of its input, so that it can get better understanding of output response In this comparator two latch has been used, due to this decision making operation becomes faster .As it can see from the corresponding output graph. Here, it can see from graph that how both output charges and discharges according to supplied input. Output plot is more accurate than double tail dynamic comparator. This due to two tail present as well as two latches is present in this circuit. Extra latch provides enough current for faster decision making in comparator circuit. Transient power is also analyzed in this circuit, So that it can get brief analysis of dynamic comparator circuit with enhanced latch regeneration speed.

In Double tail dynamic comparator with enhanced latch regeneration speed circuit simulation the given sinusoidal input of 702.5mv and 607.5 mv to differential input. Here, used 1pF capacitor is used at output node. Here both output are analyzed in terms of their respective input signal. In this comparator two latches have been used, due to this decision making operation becomes faster. As it can see from the corresponding output graph. Here, it can see from graph that how both output charges and discharges according to supplied input. Output plot is more accurate than double tail dynamic comparator. This due to two tail present as well as two latches is present in this circuit. Extra latch provides enough current for faster decision making in comparator circuit. Transient power is also analyzed in this circuit, So that it can get brief analysis of dynamic comparator circuit with enhanced latch regeneration speed.

The performance comparison is illustrated in Table 1. This table gives detailed analysis of all the comparator circuits in terms of slew rate, rise time, fall time, delay and power consumption and maximum sampling frequency

Table1. Performance comparison

Design Specification	Conventional Dynamic comparator	Double tail Dynamic comparator	Doubletail comparator with enhanced latch regeneration	Proposed Comparator
Technology	180nm	180nm	180nm	180nm
Supply	0.8v	0.8v	0.8v	0.8v
Slew rate	1.3 kv/µs	3.25 kV/µs	7.61 kV/µs	7.25kV/µs
Rise time(clock)	0.08ns	0.08ns	0.08ns	0.08ns
Fall time(clock)	0.08ns	0.08ns	0.08ns	0.08ns
Delay	13.8ns	5 µs	4.2 µs	4.26 µs
Power consumption	15.54 µw	29.21µw	28.23 µw	24.64 µw
Maximum sampling frequency	800MHz	1.6GHz	2.2GHz	2.24GHz

V. Conclusion

In this paper, comprehensive delay analysis for various varieties of clocked dynamic comparators and expressions were derived and conferred. Three structures of conventional dynamic comparator, conventional double-tail dynamic comparators and double tail dynamic comparator with enhanced latch regeneration speed were analyzed. Every time when a new comparators were analyzed it has improved power and delay compared to previous one. Every comparator were designed in cadence virtuoso. It is confirmed that the delay and Power consumption of the double tail dynamic comparator with enhanced latch regeneration comparator is reduced to an excellent extent compared with the traditional dynamic comparator and double-tail comparator.

References

[1] A.H. Hassan, H. Mostafa, K. N. Salama and A. M. Soliman, "A Low-Power Time-Domain Comparator for IoT Applications," *2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*, Windsor, ON, Canada, 2018, pp. 1142-1145.

[2] Nikoozadeh, Amin, and Boris Murmann. "An analysis of la comparator offset due to load capacitor mismatch." *IEEE Transactions on Circuits and Systems II: Express Briefs* 53.12 :1398-1402 (2006).

[3] nath Mandal, Dinabandhu, et al. "Analysis and Design of Low Voltage Low Power Dynamic Comparator with Reduced Delay and Power." *International Journal of Engineering Research and General Science* 2.3 (2014).

978-1-5386-7401-7/19/$31.00 ©2019 IEEE

[4] Babayan-Mashhadi, Samaneh, and Reza Lotfi. "Analysis and design of a low-voltage low-power double-tail comparator." *IEEE transactions on very large scale integration (vlsi) systems* 22.2 : 343-352(2014).

[5] Nikoozadeh, Amin, and Boris Murmann. "An analysis of latch comparator offset due to load capacitor mismatch." *IEEE Transactions on Circuits and Systems II: Express Briefs* 53.12 (2006): 1398-1402.

[6] Ay, Suat U. "A sub-1áVolt 10-bit supply boosted SAR ADC design in standard CMOS." *Analog Integrated Circuits and Signal Processing* 66.2 : 213-221(2011).

[7] Mesgarani, Ali, et al. "Supply boosting technique for designing very low-voltage mixed-signal circuits in standard CMOS." *Proc. IEEE Int. Midwest Symp. Circuits Syst. Dig. Tech. Papers*. (2010).

[8] Ay, Suat U. "A sub-1áVolt 10-bit supply boosted SAR ADC design in standard CMOS." *Analog Integrated Circuits and Signal Processing* 66.2: 213-2212 (2011).

[9] Blalock, B. J., et al. "Body-driving as a low-voltage analog design technique for CMOS technology." *Mixed-Signal Design, 2000. SSMSD. 2000 Southwest Symposium on*. IEEE, (2000).

[10] Goll, Bernhard, and Horst Zimmermann. "A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65 V." *IEEE Transactions on Circuits and Systems II: Express Briefs* 56.11: 810-814 (2009).

[11] Maymandi-Nejad, Mohammad, and Manoj Sachdev. "1-bit quantiser with rail to rail input range for sub-1 V ΔΣ modulators."

[12] S. U. Ay, "A sub-1 volt 10-bit supply boosted SAR ADC design in standard CMOS, Int." *J. Analog Integr. Circuits Signal Process*. vol. 66, no. 2, pp. 213–221 (2011).

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Application Specific Instruction Set Processor Design for Embedded Application Using The CoWare Tool

Lopamudra Samal
Department of ECE
SSGMCE ,Shegaon, India
lopamudrasamals@gmail.com

Chiranjibi Samal
Department of EE
NIT Rourkela,India
Chiranjibi.samal@gmail.com

Abstract— **An Application Specific Instruction Set Processor (ASIP) is widely used as a System on a Chip (SoC) Component. ASIPs possess an instruction set which is tailored to benefit a specific application. Such specialization allows ASIPs to serve as an intermediate between two dominant processor designs styles-ASICs which has high processing abilities at the cost of limited programmability and Programmable solutions such as FPGAs that provide programming flexibility at the cost of less energy efficiency. In this dissertation the goal is to design ASIP, keeping in mind a temperature sensor system. The platform used for processor design is LISA 2.0 description language and processor designing environment from CoWare. CoWare processor designer allows processor architecture to be defined at an abstract level and automatic generation of chain of software tools like assembler, linker and simulator for functional verification followed by RTL level description. RTL level description is used to generate synthesized report of the design using RTL compiler and finally the layout is created using Cadence encounter.**

Keywords— ***32-bit embedded processor; Language for Instruction Set Architecture (LISA);CoWare; Register Transfer Level (RTL); XILINX; Cadence RTL compiler; Cadence Encounter;***

I. INTRODUCTION

Wireless sensor networks (WSN) consist of a large number of wireless sensor nodes deployed randomly in the area. The nodes collect the environmental data and send them through the network towards the sink node. The nodes are constructed to be operational for a long time without replacing the batteries. Therefore, one of the primary goals when designing sensor nodes is to reduce the power consumption. To minimize the power of a sensor node, researchers tend to combine novel architecture solutions with advanced power saving techniques. In [1], authors proposed an application specific architecture that integrates an event processor that assists main microcontroller executing required system tasks. The presented approach promises good power optimization, but no real world implementation results have been presented. The approach in [2] utilizes hardware acceleration and optimized radio in a highly integrated single-chip solution. It applies an 8-bit data, 16-bit instruction CPU with reported size of 0.381 mm2 in a 0.25um process. The reduction of power in sensor node radio is also investigated. One novel approach to low power radio is presented in Pico Radio project [3]. Some researchers propose use of wake-up radio in order to reduce the radio power. Wakeup radio serves as a low-power switch to the node transceiver [4]. The implementation of advanced power-saving techniques such as dynamic voltage scaling [5] and power gating [6] promises to deliver additional reduction of node power consumption. The energy harvesting is also considered as a feasible solution to extend the battery life [7]. Using an asynchronous processor in the design of a sensor node is proposed in [8]. Another solution is an asynchronous architecture of a sensor node presented in [9]. The later solution includes additionally an energy harvesting circuit. However, no implementation results for those solutions have been presented. Fully asynchronous architecture is difficult to implement and it requires all peripherals to have a dedicated asynchronous interface.

Generally in a sensor node the processor which is used there is like a general purpose processor its area and power is not optimizes according to the application of that sensor node where as an Application Specific Instruction Set Processor (ASIP) has an instruction set optimized for a single application or a class of applications. On one hand, a DSP ASIP is a programmable machine with a certain level of flexibility, which allows it to run different software programs. On the other hand, its instruction set is designed based on specific application requirements making the processor very suitable for these applications. Low power consumption, high performance, and low cost by manufacturing in high volume can be achieved. The specialization of an ASIP provides a tradeoff between the flexibility of a general purpose CPU and the performance of an ASIC. The flexibility of these processors can be achieved by many Architecture Description Language (ADLs) like LISA, EXPRESSION etc.

The rest of this paper is organized as follows, in section II a brief discussion on types of processors are provided. The design flow of the process is briefed in section III. Processor specification and generated HDL Model is given in section IV

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Simulation results and discussion is carried out in section V and finally conclusion is given in section VI.

II. TYPES OF PROCESSORS

Processors mainly refer to the architecture of the computation mechanism employed to obtain the desired functionality of a system. The processors may be programmable or non-programmable, depending upon the application. They can be specialized and implement only a single function, or be general purpose and implement a wide range of functions. The main feature which governs the use of different types of processors for different applications are the design metrics. Some of the most commonly considered design metrics are NRE cost, flexibility, performance, power consumption, size, time to prototype and so on.

A. General Purpose Processors

A General Purpose Processor (GPP) or microprocessor as it is generally called is a programmable device that has the aim of implementing a large number of applications such that the number of devices sold is maximized. The main features of this processor are that, the program memory is not built-in to the circuit, since it has to run different programs at different times and it has a general data path, with a large register file and one or more general purpose Arithmetic and Logical Units (ALUs). It has good time-to-market and NRE costs since only the program has to be changed for the different applications without any change in hardware. Flexibility is also high due to the same reason. However, the performance is poor for certain applications and the size and power consumed are also high, because of the large hardware size.

B. Single Purpose Processors

A Single Purpose Processor (SPP) is a processor or a digital circuit which is designed to execute only a single program. For example, the circuit used for image processing in a digital camera is a SPP which has the single function of processing the input image and storing it for subsequent retrievation. It has almost the opposite features of a GPP, since it has a small register file, a dedicated data path with an ALU performing only a limited number of operations and no provision of altering the program memory. It has several design benefits, since the performance may be fast, power consumption less and also small size. However, it has the disadvantages of having very high NRE costs, low flexibility and longer design time.

C. Application Specific Instruction-set Processors

An Application Specific Instruction-set Processor (ASIP) serves as a compromise between a GPP and a SPP. It is a programmable processor which has an optimized data path for implementing only a particular class of operations. Several special functionalities may be added while unnecessary ones eliminated. Microcontrollers and Digital Signal Processors (DSPs) are some of the most common types of ASIPs in use. They have a program memory that can be changed for different applications and limited register-memory file depending upon the type of application and memory use. It has the advantages of having flexibility, at the same time achieving good performance, low power consumption and optimum size. The drawback is that it requires large NRE cost to manufacture, especially to design the compiler. Certain design environments such as CoWare offer the benefit of automatically generating the compiler which has greatly reduced the cost and time of manufacturing the device.

III. DESIGN FLOW

A. CoWare Design Flow

Fig.1 shows the flow for Coware Processor Designer Platform. The design flow concentrates on Hardware Software Co-Design. As Shown in the figure, a LISA 2.0 description of the processor is written. The Coware Processor Designer then generates software development tools. Any particular application can then be fed to these software development tools. The executable file is then analyzed using the Processor Debugger. Once the design goals are met, the synthesizable RTL can be generated. The advantage of this flow is that if the design goals are not met, we just have to change the LISA description of the processor. The processor generator does the appropriate changes in the software development tools and the RTL.

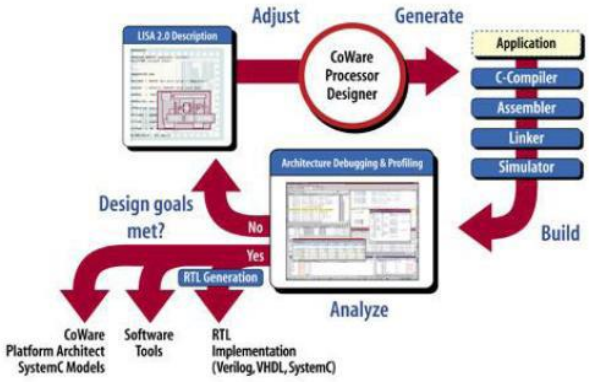

Fig.1: CoWare design ow block diagram

B. The LISA processor models

The LISA processor designer (PD) design flow was used to develop the embedded processors in this study. The LISA language supports a profile-based and stepwise refinement of processor models down to cycle-accurate and even VHDL or Verilog RTL synthesis models for fast custom VLSI implementation. Microprocessors from simple RISC to highly complex VLIW processors have been described and successfully implemented using the Processor Designer for FPGAs and cell-based ASICs. There are more than 40 LISA models in both industry and academia from different architectural categories (RISC, PDSP, and ASIP) available [12]. These include different ARM and MIPS models: PDSP from TI and StarCore, as well as ASIPs from Infineon (ICORE), STMicroelectronis, etc. LISA has been adopted by several leading ASIC houses and has over 40 members in the CoWare PD University program.

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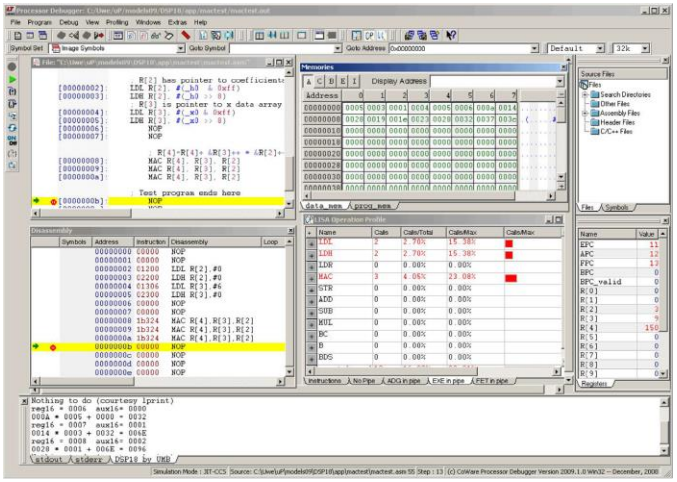

Fig.2: LISA Development tools. Disassembler (Left). Memory monitor and Pipeline pro_les (Center). Source _les and register window (Right)

C. CoWare Processor Designer

CoWare Processor Designer is an automated, application specific embedded processor design and optimization environment. The Processor Designer is the top-level model managing tool of the Processor Designer product family and is intended to facilitate designing LISA 2.0 models of processor architectures in the LISA 2.0 language. Fig.3 shows the Processor Designer Main Window. The key to Processor Designers automation is its Language for Instruction Set Architectures, LISA 2.0. In contrast to System C, which has been developed for efficient specification of systems, LISA 2.0 is a processor description language that incorporates all necessary processor-specific components such as register files, pipelines, pins, memory and caches, and instructions. It enables the efficient creation of a single golden processor specification as the source for the automatic generation of the instruction set simulator (ISS) and the complete suite of software development tools, like Assembler, Linker, Archiver and C-Compiler, and synthesizable RTL code.

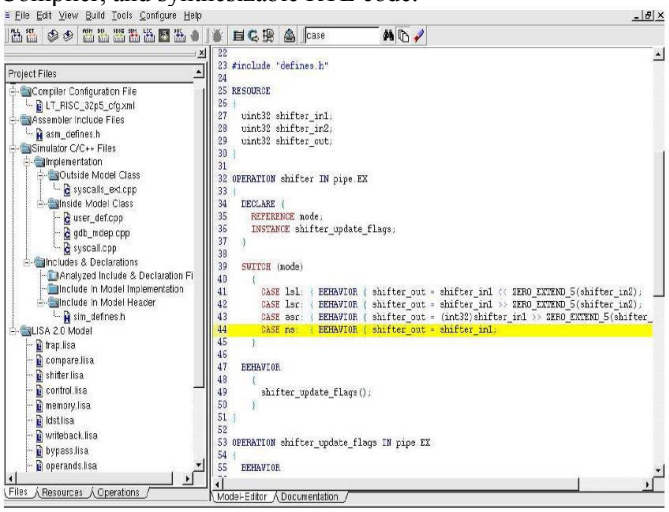

Fig 3.: CoWare Processor Designer Main Window.

D. CoWare Processor Designer

The Instruction-Set Designer is a graphical user interface (GUI) for viewing, editing, and creating LISA processor models. Having a graphical representation of a processor model rather than just the source code makes it much easier to get an overview and understand its hierarchy. Instruction sets can be designed and maintained in an intuitive way without having to cope with all the details of the syntax of the LISA language. Fig.4 shows the Instruction Set Designer Window. The Instruction-Set Designer does not replace the text editor; rather complements it. You can arbitrarily switch between the graphical and the textual representation. Changes made to the model in the GUI only result in minimal changes to the LISA code. All comments and formatted code are preserved. While the LISA hierarchy and the encoding of the instruction set is most efficiently designed with the GUI, the processors resources and the hardware behavior is still manually written as LISA code.

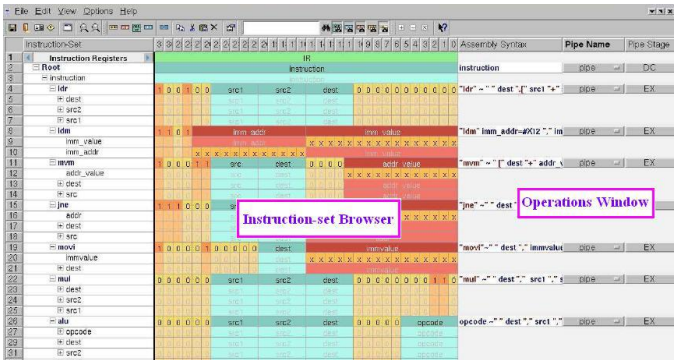

Fig .4: Instruction Set Designer Window

E. Simulation in CoWare Processor debugger

The simulation in the CoWare processor debugger can be described by following three step process Fig.5 represents that. The assembler and the linker are the standard software tools generated by the LISATek product family. An assembly file is written corresponding to the instruction set defined for the processor. The Processor Debugger GUI allows to observe, debug, and profile the executed application source code and the state of the processor by visualizing all processor resources and the output which is produced by the executed application.

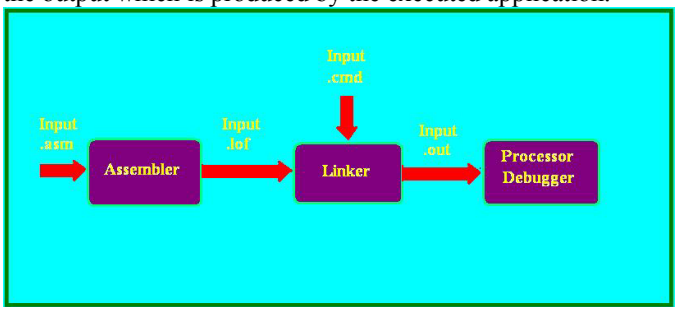

Fig.5: Simulation in CoWare Processor debugger

IV. PROCESSOR SPECIFICATION AND GENERATED HDL MODEL

A. Processor Specification Description

The designed processor is based on a 32-bit architecture with the following specifications as shown in table I. The to

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number of bits used to represent an instruction including the opcode and operands. The current instruction being executed is stored in the instruction register (IR). Eight GPRs each 32 bits in length have been defined to store any transient data required by the program. Each memory location is 19-bits in length i.e., same as that of a GPR and hence data can be transferred from memory to GPR in just one clock cycle. The defined range is 0x0000-0x8FFF (0x9000 locations). A computer program is, in essence, a stream of instructions executed by a processor. These instructions can be recorded and combined into groups which are then executed in parallel without changing the functionality of the program. This is known as instruction-level parallelism and implemented through pipelining. The designed architecture implements a 3-stage pipeline. The three stages comprise of stages like FE (Fetch and Decode), DC (Address Generation) and EX (Execution).

TABLE I: PROCESSOR SPECI_CATION

Instruction Length	32 bits
Opcode Length	8 bits
GPR	32 bits
Program Counter	32 bits
Pipeline Stages	3
Program Memory	32 bits
Program Memory Range	0x0000-0x0FFF
Data Memory	19 bits
Data Memory Range	0x0000-0x0FFF

B. The Generated HDL Model Structure

The Processor Generator tool provided in the Processor Designer generated the synthesizable RTL for both the processors. The structure of the generated HDL is given in the Fig.6 Resource model and memory model of LISA tells the information about register, memory configuration, pipeline sets and pipeline registers. To generate the base structure of a HDL model this information is used. Different entities are there in the base structure for the register resources, memory resources and the pipeline. To model the register behavior the register resources are completely generated at RTL level. As the memory entity is left empty the designer has the freedom to place any desired memory model into this entity.

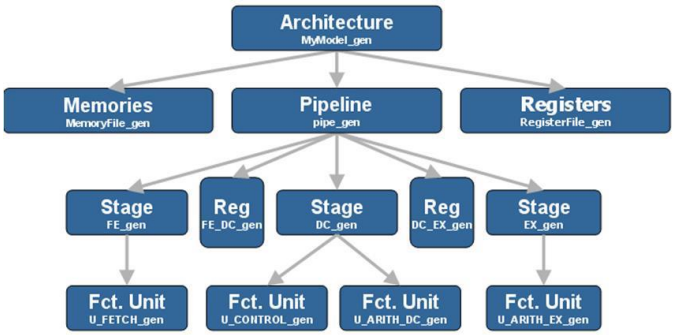

Fig.6: HDL Code Structure

V.[n] SIMULATION AND RESULTS

A. Comparison of the HDL codes generated

The HDL codes generated from the two different processors. This gives the idea about the number of lines of code of the HDL models it has been observed that the HDL code of our optimized model has very less number of lines compared with that of the previous processor(without optimization). Then both the processors have been compared with their design summery estimated value as The HDL code generated was synthesized using Xilinx ISE10.1.03. Table II show the difference.

TABLE II: COMPARISON OF TWO PROCESSORS

Device Utilization Summary (estimated values)		
Logic Utilization	**Processor 1**	**ASIP**
Number of Slices	8528	2573
Number of Slice Flip Flops	1200	887
Number of 4 input LUTs	16412	4983
Number of bonded IOBs	2	214
Number of MULT18X18SIOs	6	3
Number of GCLKs	1	1

B. Simulation Results using Xilinx ISE

All the blocks of the processor are simulated individually using Xilinx ISE Fig.7 represents the top-module simulation result

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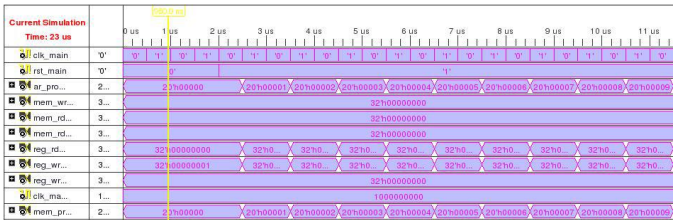

Fig. 7: simulation result using Xilinx ISE

C. Power And Area Analyses Report

Power is find out from the power analyses report of the circuit and it is 86.5202 W. Area is find out from the area analyses report of the circuit and it is found out that the area of the circuit is 43765 square micron.

D. Layout of the ASIP

The lay out of the processor is generated Cadence Encounter(Cadence-IC5141 UMC180nm technology) and Statistics for net list and Complete Global Routing report is generated. The Fig.8 shows the layout.

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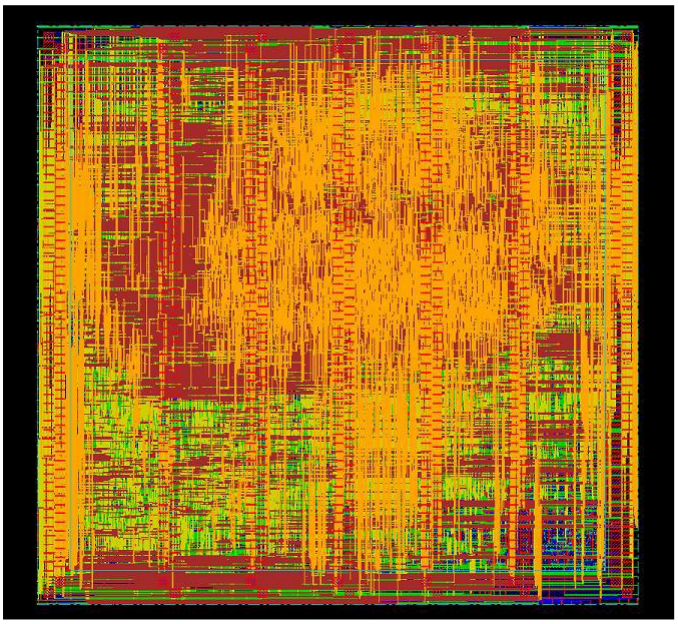

Fig.8: Layout of the ASIP

VI. CONCLUSION

Application Specific Instruction-Set Processor whose instructions were tailored made for a specific application is discussed here. This processor processed different temperature data of different areas and show the highest temperate with the location of that area. The simulation of this design was carried out on CoWare Processor Debugger platform. LISA code used to describe the architecture of this processor and CoWare tool generated HDL structure. Following the simulation work and layout was generated in Cadence encounter. This design has a three stage pipelined. using LISA and the CoWare Processor Designer Platform a processor model was implemented. The processor includes arithmetic, branch, logical and data transfer instructions. The functionality of all the instructions was checked and found to be correct using Processor Debugger. The same model was then optimized to an ASIP, According to the profiling results, the optimization was with respect to resources like data memory, program memory, instruction set and number of general purpose registers. The RTL for both the processors was generated and synthesized. The synthesis results were compared and ASIP was found to be much better than the general purpose processor in terms of power, area, memory used and lines of HDL code generated. Thus the CoWare design was explored. By considering the profiling any ASIP can be implemented and optimized taking our general purpose processor as a reference.

REFERENCES

[1] G M. Hempstead, N. Tripathi, P. Mauro, G.-Y. Wei, and D. Brooks, \An ultra low power system architecture for sensor network applications," Proc. 32nd Annual International Symposium on Computer Architecture, Madison (USA) 2005, pp. 208-219.1.

[2] J. L. Hill, System Architecture for Wireless Sensor Networks, PhD Thesis. Berkeley, CA: University of California, 2003.

[3] J. M. Rabaey, J. Ammer, T. Karalar, S. Li, B. Otis, M. Sheets, and T.Tuan, "PicoRadios for wireless sensor networks: The next challenge in ultra-low-power design," Digest Tech. Papers IEEE International SolidState Circuits Conference, San Francisco (USA) 2002, pp. 200-201.Y.

[4] L. Gu and J. A. Stankovic, "Radio-triggered wake-up capability for sensor networks," Proc. JOth IEEE Real-Time and Embedded Technology and Applications Symposium, Toronto (Canada) 2004, pp. 27-36.

[5] T. Burd, T. Pering, A. Stratakos, and R. Brodersen, "A dynamic voltagescaled microprocessor system," IEEE J. Solid-State Circuits, vol. 35, pp. 157 1- 1580,2000.

[6] G. Panic, D. Dietterle, Z. Stamenkovic, "Architecture of a Power-Gated Wireless Sensor Node," dsd, pp.844-849, 2008 lith EUROMICRO Conference on Digital System Design Architectures, Methods and Tools, 2008

[7] R. Amirtharajah and A. P. Chandrakasan, "Self-powered signal processing using vibration-based power generation," IEEE J. Solid-State Circuits, vol. 33, pp. 687- 695, 1998.

[8] C. Kelly, IV , V. Ekanayake , R. Manohar, SNAP: A Sensor-Network Asynchronous Processor, Proceedings of the 9th International Symposium on Asynchronous Circuits and Systems, p.24, May 12- 15, 2003

[9] Y. Ammar , A. Buhrig , M. Marzencki , 8. Charlot , S. Basrour , K. Matou , M. Renaudin, "Wireless sensor network node with asynchronous architecture and vibration harvesting micro power generator," Proceedings of the 2005 joint conference on Smart objects and ambient intelligence: innovative context-aware services: usages and technologies, October 12- 14,2005, Grenoble, France.

[10] A Ho_mann, T Glo Kler and H Meyr', "Methodical low-power asip design space exploration", pages 229- 246. Journal of VLSI Signal Processing, Kluwer Academic Publishers, 2003.

[11] Et al. M. Itoh. Peas-iii: An asip design environment. pages 430- 436. IEEE Int. Conf. on Computer Design: VLSI in Computers and Processors, 2000.

[12] LISA Language Reference Manual supplied by CoWare.

[13] J. H. Yang et al. Metacore: An application-specific programmable dsp development system. pages vol.8 no.2,173- 183. IEEE Transactions on Very Large Scale Integration Systems, April 2000.

[14] P. Russo G. Hadjiyiannis and S. Devadas. A methodology for accurate performance evaluation in architecture exploration. New Orleans, 36th Design Automation Conference, June 1999.

[15] A. Nicolau F. Onion and N. Dutt. Incorporating compiler feedback into the design of asips. pages 508- 513. Proc. of European Design and Test Conference, 1995.

[16] R. Leupers. Retargetable Code Generation for Digital Signal Processors.Kluwer Academic Publishers, 1997.

[17] L. Samal, K. K. Mahapatra and K. Raghuramaiah, "Class-C power amplifier design for GSM application," *2012 International Conference on Computing, Communication and Applications*, Dindigul, Tamilnadu, 2012, pp. 1-5.doi: 10.1109/ICCCA.2012.6179216

[18] L. Samal and C. Samal, "Designing a low power 8-bit application specific processor," *2014 International Conference on Green Computing Communication and Electrical Engineering (ICGCCEE)*, Coimbatore, 2014, pp. 1-5.doi: 10.1109/ICGCCEE.2014.6922238.

[19] http://ethesis.nitrkl.ac.in/view/people/

[20] A. Hofiman, F. Friedler, A. Nohl and Surender Parupalli. A Methodology and Tooling Enabling Application Specific Processor Design. In Proc. of the VLSID, 2005

[21] Li Zhang, Shuangfei Li, Zan Yin andWenyuan Zhao. A Research on an ASIP Processing Element Architecture Suitable for FPGA Implementation.In Proc. of the International Conference on Computer Science and Software Engineering, 2008.

[22] V. Ekanayake, C. Kelly, et al., An Ultra Low-Power Processor for Sensor Networks., ASPLOS04, October 2004.

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Analysis of Electroencephalogram for Cognitive Effects of Human Being Before and After Meditation

Manish N. Tibdewal
Department of Electronics and Telecommunication Engineering
Shri Sant Gajanan Maharaj College of Engineering, SHEGAON, 444203, MAHARASHTRA, INDIA
mntibdewal@ssgmce.ac.in

Dhanashri N. Nagbhide
Department of Electronics and Telecommunication Engineering
Shri Sant Gajanan Maharaj College of Engineering, SHEGAON, 444203, MAHARASHTRA, INDIA
dhanashri4nagbhide@gmail.com

Kanchan B. Thakare
Department of Electronics and Telecommunication Engineering
Shri Sant Gajanan Maharaj College of Engineering, SHEGAON, 444203, MAHARASHTRA, INDIA
thakarekanchan15@gmail.com

***Abstract*— The meditation is significantly suggested by the medical practitioners and health care organization for the individuals to relieve the stress and pain. The meditation has severe impact of human beings brain functions. Thus, it is required to analyze the neuro-cognitive effects of meditation using the more effective tool called Electroencephalogram (EEG) to record the brain activities of meditators. In this paper, it is analyze the EEG for neuro-cognitive effects on human being for before and after a month of meditation intervention for 15 subjects. The EEG analysis is done using the energy spectral analysis, statistical and spatial features. From the analysis it is found that, the variance for before meditation (16.8133) is higher and variance for after meditation (7.4628) is lower. Mahalanobis distance for before meditation (0.0848) is lower and for after meditation (0.1537) is higher. The *p*-value is less than significance level ($p < 0.05$) for both features indicating that, good discrimination between control and meditators group. The Delta, alpha and theta rhythms' energy increases in EEG after meditation. It is observed that after a month of regular meditation, increases alpha and theta energy in a frontal lobe. Hence relaxation improves after meditation and the brain cognitive function excel in meditators.**

Keywords*— EEG, meditation, Variance, Mahalanobis distance, p-value, Energy spectral density

I. INTRODUCTION

EEG signals are the signatures of neural activities. Since long time, the meditation practices followed by the human beings to address the various health related problems. Basically the meditation is activity that helps deepen understanding of the sacred and mystical forces of the life. To analyze effects of meditation using the important monitoring technique called Electroencephalography to record electrical activity of human cerebrum. In current days, significant amount of mental stress due to hectic work schedules is leading to insomnia, negative emotions, depression, life spoiling diseases and many other symptoms after an extended period. Previous researchers showed that meditation can significantly affect physical and mental relaxation and found out the effect of meditation on stress relief and disease declination [1], [2]. EEG signals are considered to be non-stationary, random, and non-linear in nature. The important features of these signals can be determined by time-frequency analysis. In relation with the EEG signals, a lot of work has been done to find the significant changes between the signals and the mental states by using different advanced signal processing techniques. EEG studies have utilized these methods to portray the brainwave changes that occur in meditation [3]. Although the meditative changes in EEG signals have not yet been firmly established, the preliminary findings have implicated increases in theta and alpha band power and decreases in overall frequency [4]. Ahmed et al. presented Time-frequency analysis using DWT [5]. Ahani et al. proposed the techniques of EEG processing and respiration signals by using Support Vector Machine (SVM) and spectral analysis [6]. Mingqian et al. designed the questionnaires were to analyze the meditation depth and brain activities recorded with EEG [7]. Oldrichet al. computed the fractal dimension and permutation entropy as features to detect calming and insight meditation in electroencephalographic (EEG) signals using Sevcik's algorithm [8]. Fulpatil et al. presented the study to obtain new insights into the nature of EEG during meditation; the recorded signals were analyzed using wavelet transform [9]. Andrew et al. presented the theoretical-conceptual presented the discussion of the problem and presents some illustrative results on the usage of EEG screening for the guidance of mediation personalization [10]. Chandana et al. proposed approach to trace the varying spectral characteristics of EEG during meditation and then the changes of EEG signals during meditation using quantitative analysis [11]. Traisak et al. presented work to observe effect of a piano music mixed with a 5 Hz (theta band enhancement) binaural beat frequency was used to modulate the brain signals continuously for seven days [12]. Kaur et al. presented the broad spectrum of neural mechanics under a variety of meditation effects based on changing EEG brainwave patterns [13]. Sharma et al. investigated the effect of regular meditation practice on EEG brain dynamics in low frequency bands of long-term Rajyoga meditators [14]. Mariappan et al. proposed to experimental investigation of the impact of Rajyoga meditation on physical and mental health using statistical analysis and t-test [15].

In this work, the aim is to analyze the neuro-cognitive effects of meditation on human beings using the recorded EEG signals for before and after a month of meditation for 15 subjects with different age and gender. The novelty is in study is that; the analysis is done using the energy spectral analysis, statistical and spatial features. The analysis performed in different ways such as- time-domain analysis of EEG signals for before and after mediation, statistical and spatial analysis of 15 meditators using the features: Variance

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and Mahalanobis distance. Spectral analysis is performed through energy spectral density for one subject before and after a month of meditation intervention.

II. Methods And Material

In this project the 'Medicaid Neuro-Compact 2400' system is used to acquire EEG signal from different subjects using Ag-Cl types of electrodes for investigating the impact of meditation. There are total 19 electrodes data acquisition systems with 10-20 international system. (The channels: FP1, FP2, F7, F3, Fz, F4, F8, T3, C3, Cz, C4, T4, T5, P3, Pz, P4, T6,O1,O2) The sampling frequency Fs is 114 Hz. EEG signal recording is done before meditation and after a month meditation intervention. Before meditation EEG data recorded by requesting the subjects to be relaxed their mind for 5 Min. The same subjects have performed continuously meditation for minimum 10 Minute daily for a month. After a month of meditation intervention EEG was recorded for 5 Minute.

The prefrontal cortex is responsible for cognitive process [7]. Thus for analyze the neuro-cognitive effects of meditation the frontal lobe electrodes are used (F3, F4, F7, F8, FP1, FP2, Fz). The statistical, spectral and spatial analyses are performed by using Variance; Standard deviation; Mahalanobis distance features and energy spectrum. All the recorded data set are processed using the MATLAB R2013a platform. The equations for computation of each of these features are demonstrated as below.

Standard Deviation: The Standard Deviation (σ) is the estimation of the mean square deviation of electrical activity (x_i) from its mean value. Standard deviation describes the dispersion within a local region. The standard deviation of EEG signal is evaluated as shown in Equation (1).

$$\sigma = \sqrt{\frac{1}{n}\sum_{i=0}^{n}(x_i - \mu)} \quad (1)$$

where (x_i) = Electrical activity of brain, μ = Mean (Average),
n = Number of samples of one epoch.

Variance (Var): The variance measures the variability of electrodes potential. It is computed by using standard deviation (σ) as given in (2).

$$Var = \sigma^2 \quad (2)$$

Variance shows the variability of electrodes potential from the mean value. As the variability electrodes potential low from its mean value then subject get relaxed. The variance calculated through all four bands of EEG (Alpha, Beta, Theta, and Delta) after averaging frontal electrodes for before and after a month of meditation intervention.

Mahalanobis Distance: Mahalanobis distance is the distance between a point and a distribution. And not between two distinct points, it is effectively a multivariate equivalent of the Euclidean distance. The Mahalanobis distance introduced to overcome the problems of Euclidean distance. The Mahalanobis distance of each EEG signal is computed given in (3).

$$D^2 = (x - m)^T \times C^{-1} \times (x - m) \quad (3)$$

D^2 : The square of the Mahalanobis distance.
x : The vector of the observation (row in a dataset),
m : The vector of mean values of independent variables (Average of each column),
C^{-1} : The inverse covariance matrix of independent variables.

Energy Spectral analysis: The Energy Spectral Density (ESD) has calculated using FFT that shows the strength of variation as function of frequency which quantify the amount of energy in a different frequency band. Spectral analysis provides information about the presence of different frequencies in EEG signal, which reflects the general arousal levels of brain. The rhythmic nature of many EEG activities explains need for spectral analysis. The FFT allows separating different rhythms and estimating their frequency of each other. The energy spectrum is evaluated through FFT by averaging of all the channels of frontal lobe.

The EEG data of each subject processed using band pass filter in 1 to 30 Hz. This band pass filter designed using FIR filter. The Energy Spectral Density (ESD) feature is used for frequency-energy analysis. This feature estimated at the frontal electrode various bands, including delta (0.5-4Hz), theta (4-8Hz), alpha (8-12Hz), beta (12-30Hz). The spectral analysis has performed for one subject before and after meditation. The ESD feature estimation process flow diagram for before and after meditation is shown in fig. 1.

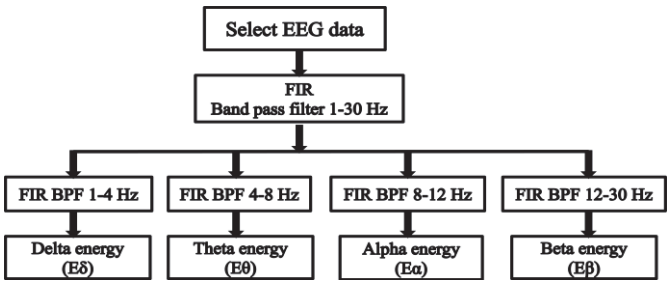


Fig. 1. ESD feature estimation process flow diagram

III. Experimental Results

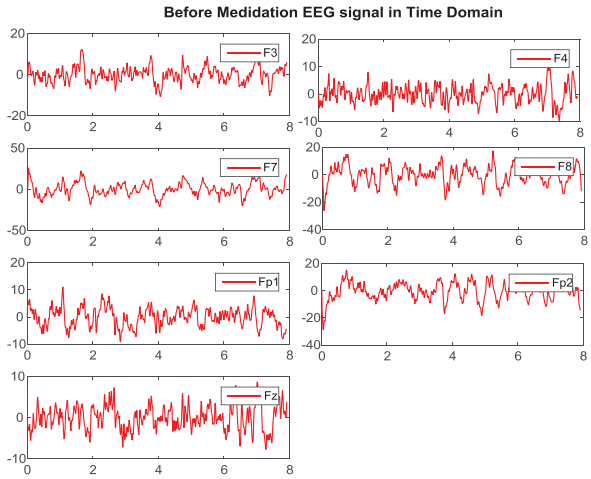
According to the methodology used, each subjects' EEG signals are analyzed for before and after meditation. In the fig. 2, frontal lobe channels F3, F4, F7, F8, FP1, FP2 and Fz demonstrated the EEG signals before and after meditation using time domain analysis for one subject. X-axis denotes time (sec.) and Y-axis denotes amplitude (micro-volt). Both the representations show the variations and changes in EEG signals for all the frontal lobe EEG channels.

Table 1, presented the minimum and maximum amplitudes of all frontal lobe channels for one subject. All minimum values are negative and all maximum values are positive. From the analysis, it is observed that average minimum and maximum values of amplitudes are -16.17 and 14.64 respectively for before meditation. And average minimum and maximum values of amplitudes are -15.23 and 11.14 respectively for after meditation. It is inferred that after meditation the EEG signals' magnitudes are lowered compared to before meditation.

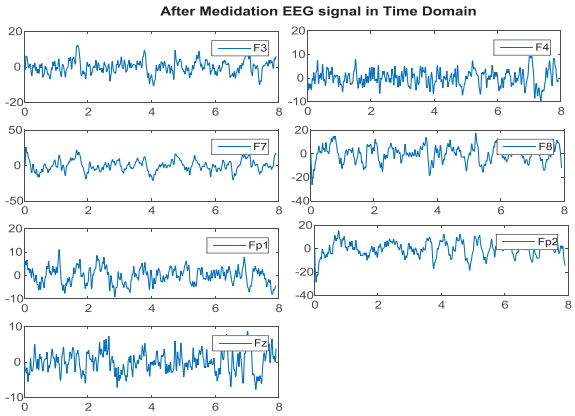
TABLE I. MINIMUM AND MAXIMUM AMPLITUDES OF ALL FRONTAL LOBE CHANNELS FOR ONE SUBJECT

	F3		F4		F7		F8		FP1		FP2		Fz		Avg. Amplitude	
Channel (s)	**B**	**A**	**B**	**A**	**B**	**A**	**B**	**A**	**B**	**A**	**B**	**A**	**B**	**A**	**B**	**A**
Min. Amplitude(μV)	-10.76	-12.20	-9.64	-10.26	-21.12	-30.27	-26.16	-18.79	-9.15	-12.43	-28.67	-14.38	-7.72	-8.30	-16.17	-15.23
Max. Amplitude(μV)	12.29	9.28	11.45	7.94	26.03	16.84	17.51	14.84	11.13	9.65	15.38	12.11	8.74	7.32	14.64	11.14

(B = Before meditation, A = After a month of meditation intervention)



(a) Before meditation EEG signal in time domain



b) After meditation EEG signal in time domain

Fig. 2. Time domain analysis of frontal lobe for a subject for before and after meditation

This study estimate the statistical and spatial analysis after averaging the 7 channels data, it demonstrated features such as variance, and Mahalanobis distance. For all 15 subjects we measured variations in the meditation effects of human being using EEG signals. Table 2, shows the statistical and spatial analysis for all 15 subjects using before and after meditation. It is found that, the variance for before meditation (16.8133) is higher and variance for after meditation (7.4628) is lower also Mahalanobis distance for before meditation (0.0848) is lower and Mahalanobis distance for after meditation (0.1537) is higher. Fig. 3 and fig. 4 depicted the bar graph of variance and Mahalanobis distance respectively.

TABLE II. STATISTICAL AND SPATIAL ANALYSIS FOR BEFORE AND AFTER MEDITATION

Subjects(S) /Gender/ Age	**Variance**		**Mahalanobis distance**	
	Before meditation	**After a month meditation intervention**	**Before meditation**	**After a month meditation intervention**
S1/M/28	15.2154	7.8781	0.0661	0.1453
S2/F/19	12.2390	7.9882	0.0821	0.1293
S3/F/19	6.5703	6.4904	0.1536	0.1541
S4/F/22	4.4165	3.3010	0.2264	0.3035
S5/M/32	13.9722	5.6690	0.0718	0.1786
S6/M/29	22.9541	11.1701	0.0463	0.1031
S7/F/22	11.6800	7.6930	0.0862	0.1302
S8/F/23	12.6370	9.8067	0.0819	0.1031
S9/F/22	48.9391	12.6757	0.0214	0.0791
S10/F/50	15.8281	6.0260	0.0635	0.1676
S11/F/18	29.7512	10.0489	0.0339	0.0996
S12/M/30	11.0975	5.4164	0.0916	0.1854
S13/F/19	23.5830	7.1708	0.0446	0.1395
S14/F/18	16.1952	5.8808	0.0620	0.1723
S15/F/19	7.1213	4.7269	0.1405	0.2143
Average	16.8133	7.4628	0.0848	0.1537

In this paper, the student t-test is used to observe the significant difference between the before and after a month of meditation intervention EEG data. The student t-test, it is hypothesis that 'there is no difference in average of two data sets' [16]. It is depicted that, if the *p*-value is equal or less than significance level, it shows that there is higher discrimination between two data sets. The *p*-value evaluated from student t-test by choosing variance feature with 0.05 as the significance level. From this test, the *p*-value for variance is $0.00079 \ll 0.05$ and *p*-value for Mahalanobis distance is $0.0000004 \ll 0.05$. Hence it is inferred that, resulted lower *p*-value has higher discriminating data set between before and after a month of meditation intervention.

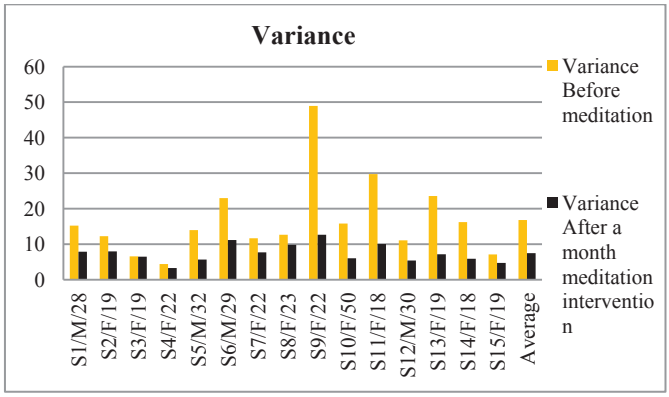


Fig. 3. Bar graph of Variance for before and after meditation

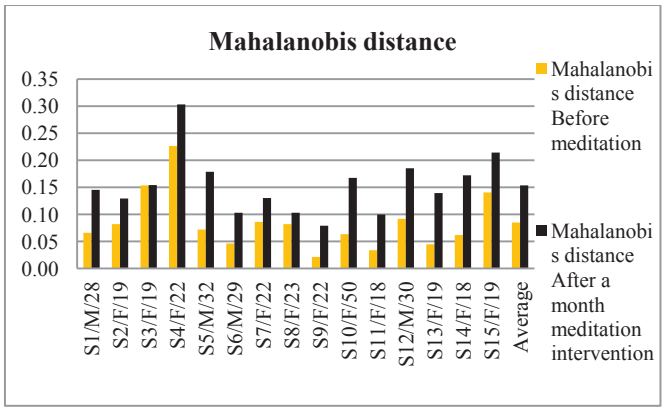
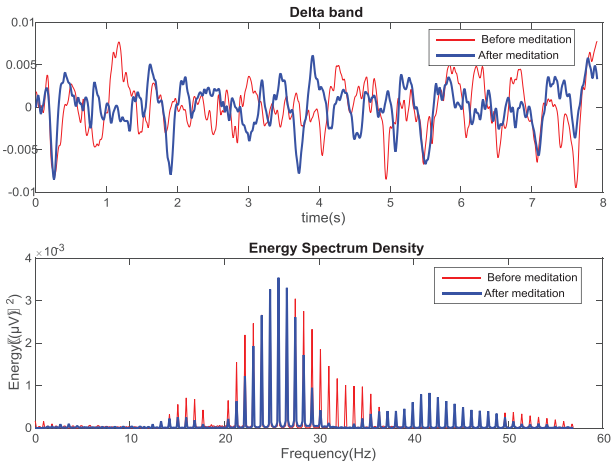


Fig. 4. Bar graph of Mahalanobis distance for before and after meditation

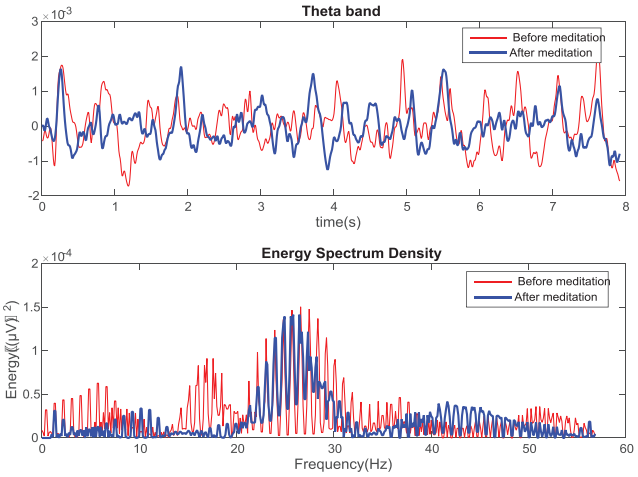
From the results it is noticed that the variance value is higher before the meditation than the after meditation which mean that reduces the stress and anxiety on subject brains. The Mahalanobis distance is increased after the meditation so brain activities of the meditators relaxed which is differ from the brain activities recorded before the meditation. The average values show the significant changes in EEG signals after the meditation practices in order to justify the effects of meditation on human being brain activities.

Energy Spectral Analysis: The purpose of this work is to estimate the effects on human being after the meditation. This is done by investigating the different brain rhythms. The energy spectrum is evaluated through FFT by averaging of all the channels of frontal lobe. Fig.5 presented the each rhythms and their ESD for a subject. Fig.5(a) shows the delta rhythm and ESD, fig.5(b) shows the theta rhythm and ESD, fig.5(c) shows the alpha rhythm and ESD and fig.5(d) shows the beta rhythm and ESD.

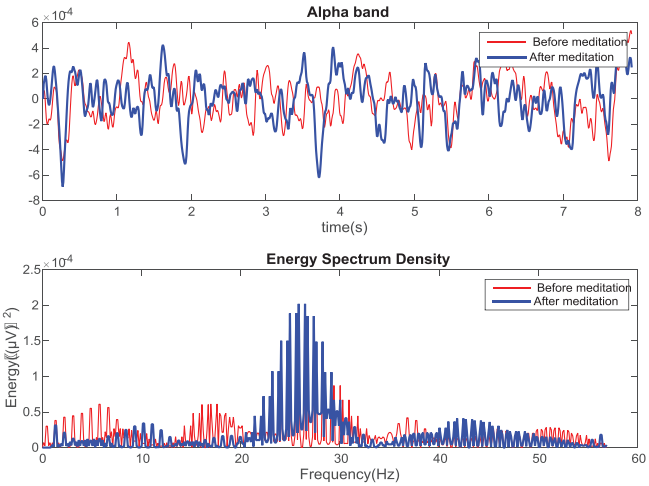
From the energy spectral analysis it is found that delta, alpha and theta bands shows an overall increase in energy after meditation. Whereas, beta band energy decreased in same subject. Improved energy value in alpha band indicates that the person is alert to the external word, even when the person is meditating [11].Thus increase in alpha and theta parameter showed the relaxation in after meditation and enhance cognitive effects in meditators.



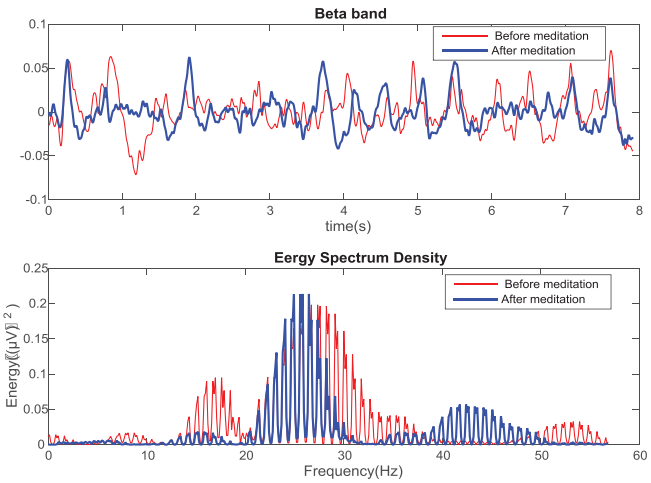
(a) Energy spectrum of delta rhythm before and after meditation



(b) Energy spectrum of theta rhythm before and after meditation



(c) Energy spectrum of alpha rhythm before and after meditation



(d) Energy spectrum of beta rhythm before and after meditation

Fig. 5. Energy Spectral analysis of all frontal lobe channels for before and after meditation

IV. DISCUSSIONS AND CONCLUSION

The prefrontal cortex is responsible for the cognitive processes as problem solving, attention interactions with other brain parts, which also sensitive to acute and chronic stress. For a changed pattern of frontal functioning might be expected in subjects reporting a greater sense of self during activity. In this work frontal lobe channels used for analyzing the cognitive effects of human being. The work presented that analyzes the effects of before and after a month of meditation intervention. While investigating the work in order to analyze the impact of meditation that shows the variance values are higher before the meditation than after meditation. It means that reduces the stress level and anxiety of subjects.

The Mahalanobis distance is increased after the meditation of the participants. The subjects are relaxed compared to the brain activities recorded before the meditation. The student t-test is used to observe the significant difference between the before and after a month of meditation intervention EEG data. The resulted lower *p*-value has higher discriminating data set between before and after a month of meditation intervention. In the energy spectral analysis it is observed that, each rhythm's energy has got significant changes in after meditation. From this analysis after a month of meditation in meditators revealed a generalized increase in theta energy which related with the mental consciousness and increases the cognitive function. The alpha energy after meditation in meditators also increases it correlated with lower levels of anxiety and positive effects. In summary, alpha band energy increases are related to relaxation, which is observed in energy spectral. Thus, meditation improves cognitive function and increase in mental concentration as evidence by increased in alpha and theta energy in a frontal lobe. It is implicated that increase in alpha and theta bands energy, decreased in overall frequency. Hence it is inferred that, increase in alpha and theta bands' energy, increases the non-linearity of EEG. Therefore relaxation improves after meditation and the brain cognitive function in meditators which justifies the meditation effects. For the future work it is needed to investigate more features by using more subjects and with sustained period of meditation for better results.

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REFERNCES

[1] Wang, Shih-Feng, Yu-Hao Lee, Yung-Jong Shiah, and Ming-Shing Young. "Time-frequency analysis of eegs recorded during meditation." In 2011 First International Conference on Robot, Vision and Signal Processing, pp. 73-76. IEEE, 2011.

[2] Meditation Practices for Health: State of the Research Evidence Report/Technology Assessment, No. 155, University of Alberta Evidence-based Practice Center Edmonton, Alberta, Canada, AHRQ Publication No. 07-E010, June 2007.

[3] On, F. R., R. Jailani, H. Norhazman, and N. Mohamad Zaini. "Binaural beat effect on brainwaves based on EEG." In 2013 IEEE 9th International Colloquium on Signal Processing and its Applications, pp. 339-343. IEEE, 2013.

[4] Subha, D. Puthankattil, Paul K. Joseph, Rajendra Acharya, and Choo Min Lim. "EEG signal analysis: a survey." Journal of medical systems 34, no. 2 (2010): 195-212.

[5] Ahmed, Tazrin, Monira Islam, Md Salah Uddin Yusuf, and Mohiuddin Ahmad. "Wavelet based analysis of EEG signal for evaluating mental behavior." In 2013 International Conference on Informatics, Electronics and Vision (ICIEV), pp. 1-6. IEEE, 2013.

[6] Ahani, Asieh, Helane Wahbeh, Meghan Miller, Hooman Nezamfar, Deniz Erdogmus, and Barry Oken. "Change in physiological signals during mindfulness meditation." In 2013 6th International IEEE/EMBS Conference on Neural Engineering (NER), pp. 1378-1381. IEEE, 2013.

[7] Liu, Mingqian, and Nugraha Priya Utama. "Meditation Effect on Human Brain Compared with Psychological Questionnaire." International Journal of Information and Education Technology 4, no. 3 (2014): 264.

[8] Vyšata, Oldřich, Martin Schätz, Jakub Kopal, Jan Burian, Aleš Procházka, Kuchyňka Jiří, Jakub Hort, and Martin Vališ. "Non-Linear EEG measures in meditation." Journal of biomedical science and engineering 7, no. 09 (2014): 731.

[9] Fulpatil, Prajakta, and Yugandhara Meshram. "Review on Analysis of EEG Signals with the Effect of Meditation." Int. Journal of Engineering Research and Applications June (2014).

[10] Fingelkurts, Andrew A., Alexander A. Fingelkurts, and Tarja Kallio-Tamminen. "EEG-guided meditation: a personalized approach." Journal of Physiology-Paris 109, no. 4-6 (2015): 180-190.

[11] Chandana, Vijayalakshmi, Vinod Kochupillai, "Quantitative Analysis of EEG Signal Before And After Sudharshana Kriya Yoga," International Journal Of Public Mental Health And Neurosciences, pp.19-21,Volume 2, Issue 2, August -2015.

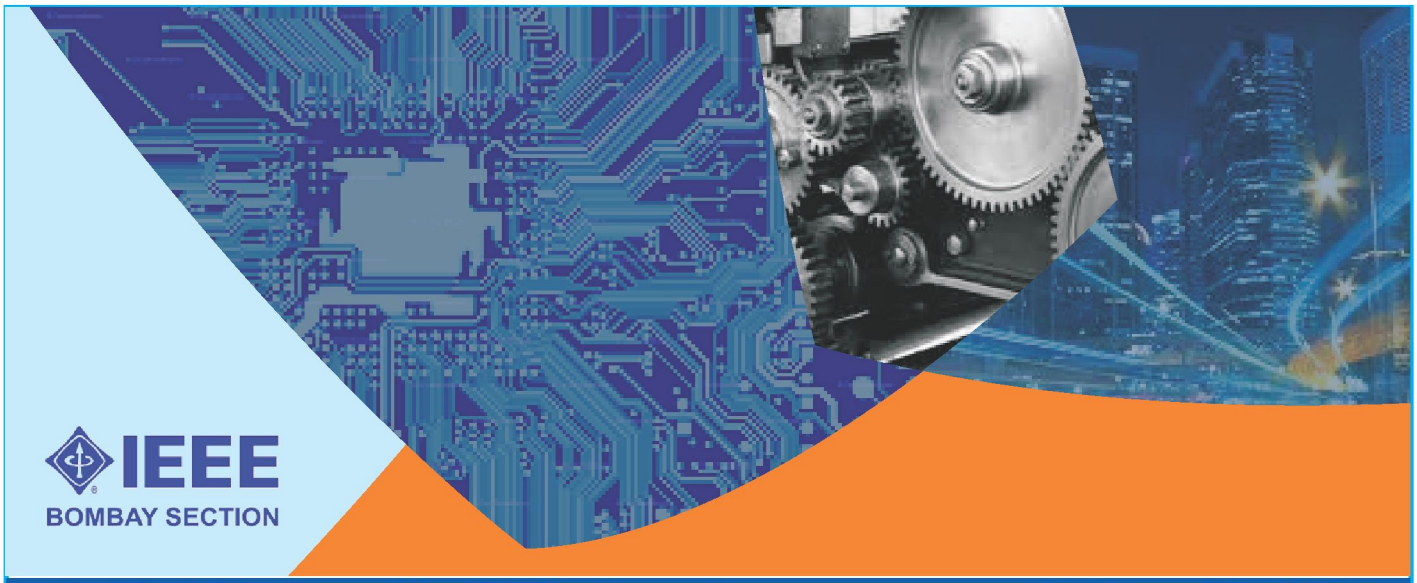
[12] Yamsa-Ard, Traisak, and Yodchanan Wongsawat. "The observation of theta wave modulation on brain training by 5 Hz-binaural beat stimulation in seven days." In 2015 37th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), pp. 6667-6670. IEEE, 2015.

[13] Chamandeep Kaur and Preeti Singh, "EEG Derived Neuronal Dynamics during Meditation: Progress and Challenges," Adv Prev Med. 2015; 2015: 614723.

[14] Sharma, Kanishka, Sushil Chandra, and Ashok Kumar Dubey. "Exploration of lower frequency EEG dynamics and cortical alpha asymmetry in long-term rajyoga meditators." International journal of yoga 11, no. 1 (2018): 30.

[15] Mariappan, Ramasamy, and M. Rama Subramanian. "Experimental Investigation of Cognitive Impact of Yoga Meditation on Physical and Mental Health Parameters Using Electro Encephalogram." In Soft Computing and Medical Bioinformatics, pp. 129-139. Springer, Singapore, 2019.

[16] Tibdewal, Manish N., Himanshu R. Dey, Manjunatha Mahadevappa, AjoyKumar Ray, and Monika Malokar. "Multiple entropies performance measure for detection and localization of multi-channel epileptic EEG." Biomedical Signal Processing and Control 38 (2017): 158-167.



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Splay: A Lightweight Video Streaming Application

Nilesh S Inkane
Department of Information Technology
Shri Sant Gajanan Maharaj
College of Engineering
Shegaon, India
inkanenilesh@gmail.com

Siddhi A Kotak
Department of Information Technology
Shri Sant Gajanan Maharaj
College of Engineering
Shegaon, India
siddhikotak0798@gmail.com

Amitkumar S. Manekar
Department of Information Technology
Professor at Shri Sant Gajanan Maharaj
College of Engineering
Shegaon, India
asmanekar24@gmail.com

***Abstract* - Splay is a video streaming progressive web application which uses YouTube as a server and storage for videos and the app itself resides on our own desired server. Splay achieves this by using embed feature provided by YouTube and hence can even be hosted on a smaller server without carrying the load of videos. It is developed to work on any given device and any given platform provided, the given device has a browser. An app shell architecture is implemented in splay with the use of service workers and JavaScript for the technology stack. It uses React.js for developing user interfaces and achieving a single page application model for the more native-like experience. Node.js and Mongo DB are the ones powering the back end of the application. This paper basically focuses on the architecture and working of the application and our main focus is to collect all important educational videos of college including lectures, tutorials on one platform with proper content management as desired by the institute or organization using it.**

Keywords—Progressive web apps, PWA, React.js, Node.js, video streaming, YouTube embed.

I. INTRODUCTION

In the world of 4.5 billion internet users and astounding internet speeds, it is easy for people to access the internet whenever they want and for whatever they need, especially videos. This has enforced most of the activities being carried online including learning. Websites like Udemy, Coursera, EDX, TED talks and YouTube are already on the top and are being used by many professionals. The most viewed platform amongst all is YouTube and allows all types of video content to be uploaded on it whereas the former ones do not and they work on a specific niche. But due to scattered content on the internet, the ability to make the audience focus on what any given institution wants lacks. Self-hosting videos is a bad idea as streaming video needs a lot of transcoding and serving them according to the client's device specifications. Users mostly access the internet through their smartphones and hence an application must load quickly and work as fast as it can.

Splay is a video streaming, progressive web application for such institutions. It uses YouTube to upload videos and embeds them on splay. YouTube servers are best at transcoding videos and providing them at their best quality and formats according to the client's device specifications and internet speed. Splay whereas provides more control over what users can see and access. Videos can be set to *unlisted* on YouTube so that they are only visible on splay. Within smaller organizations, it can play a vital role as a focused social media with more control of everything which is uploaded on splay. A simple approval system is implemented for verification of content uploaded on the application. A group of admins can be assigned to manage the content and users on the application and hence becomes a perfectly managed media app for institutions.

Splay is implemented using Javascript. It uses React.js to accomplish a single page application model and easy state management with insane speeds. The front end works without reloading the web page and renders components instead of HTML pages for each request sent. This avoids sending multiple HTTP requests to the server and saves a lot of time and makes the app faster. Back end implements are composed of MongoDB and Node js, again Javascript. A NoSQL database like MongoDB is used because it is a lot faster, easier to implement with node and flexible for future purposes.

Splay is a progressive web application or PWA, wherein progressive means for all types of users. This makes splay run on any given device and any given specification, condition, the device has a browser. PWAs implement multiple modern techniques like caching to provide faster and engaging apps.

II. RELATED WORK

A. So Why PWA?

Peixin Que, Xiao Guo and Maokun Zhu "Comprehensive Comparison between Hybrid and Native Paradigms" have explained with brief statistics and some facts about why Hybrid applications can have an edge over native apps. From here we move one step closer towards Progressive Web Apps. Mobile apps are being used for most of the tasks today and that is because smart phones are easily accessible than desktops and laptops. The sales of phones are increasing exponentially with the number being 1.3 billion in 2014 and which is also a 27.3% increase than the previous year i.e. 2013 [1]. Today, in 2019 the count is raised to 3.8 billion and still increasing. With such abundant mobile users and ever-growing need for ease of accessibility and speed, there are numerous ways to develop performant apps. Native and Hybrid apps are such two ways with Native being the applications for a particular platform and the latter run on other platforms under a container that renders HTML, CSS, Javascript. The hybrid mobile apps without a doubt are easy for developers to develop and deploy. Below Fig 2.1 shows some of the aspects of the developer's ease.

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Evaluation Criteria	Hybrid App	Native App
Programming Language	✓	×
Documents/ IDE	✓	✓
Compatibility	✓	×
Debug/ Test	✓	✓
Distribution	✓	×

Fig 2.1- Comparing native and hybrid apps as per developers

But from the user's viewpoint, they do not care about the process of development. Users care more about their experience of using the app. This is called User Experience and this is what makes the app better for users [2].

Performance Parameter	Hybrid App	Native App
Installation Consuming Time (sec)	9.37	7.64
Startup Consuming Time (sec)	1.58	1.11
CPU Occupancy Ratio(%)	11.76	5.54
Memory Occupancy (MB)	101.66	58.77
Battery Temperature (Celcius)	45.32	37.54
Network Flow (KB)	330.56	323.89

Fig 2.2- Comparing the performance of native and hybrid apps

Fig 2.2 clearly explains how the hybrid app lags behind native apps in case of performance parameters or we can say User Experience. The installation time is 22% more and the package is almost 43% larger than native apps as it is bundled with extra plugins to make the app run on the platform. But since hybrid apps save so much cost of companies and are better at development than native apps, most of the companies still prefer them over native ones[3]. This is where PWAs come to the rescue. They are directly web apps served through the web and run on any platform with the help of a browser. Since they are web apps, It is obvious they are made with HTML, CSS and JavaScript and hence cover all the advantages hybrid apps have over native apps.

Progressive Web Apps provide ease to both users and developers. They are made using only two additional files namely, manifest file and service workers. They are made with keeping in mind the app shell architecture [5]. This is the minimal HTML, CSS, JS needed for your app to run and is usually cached using service workers [5] [6]. PWAs are easily installable through browsers and are installed by pop up banners when the user first time visits the websites and not only that they are also testable even before installation [4].

B. *Technology Stack*

The application, as mentioned previously uses JavaScript for full-stack development. The application leverages react.js for user interfaces. React is a front end JavaScript library developed by Facebook in 2011. React provides better DOM or Document Object Model updating methods as it only changes the part of the DOM which has been updated and not the whole DOM which is the usual case without React. This is achieved using a concept known as virtual DOM [7]. A virtual DOM is a node tree just like the real DOM. The real DOM is not used by React as the browser needs to repaint the whole DOM for every change. However, React creates instances of virtual DOM when changes happen. Now React follows three steps to render the browser's DOM -

1. Whenever anything might have changed, the whole UI will be re-rendered in virtual DOM representation.

2. The difference between previous and virtual DOM representations will be calculated.

3. Now the real DOM will be updated as per the calculations.

With rendering speed being covered, React also helps developers to develop the UI faster with reusable components. React provides easy solutions to state management and single page applications. Back end uses Node server, which is a runtime environment for JavaScript code to run on the server side. Node was developed by Ryan Dahl in 2009 and later sponsored by Joyent. Node is an event-driven, non-blocking asynchronous run time and hence supports scalability. Node provides more control to the developers of the process running on the system. Unlike multithreading Node uses a single thread which is not vulnerable to deadlocks. It uses asynchronous I/O for multiple processes and JavaScript is best for this since it supports callbacks [8]. Splay uses MongoDB as a database with Node. MongoDB is a NoSQL, document oriented database which uses collections instead of tables and relations.

III. Experimental Setup

This section revolves around the basic functionalities of splay which are to be seen at the time of deployment. Splay usually works in Client-Server passion, whereas the commercial version of Splay is in peer to peer infrastructure base. First of all discussion is made along Use Cases where all stakeholders are considered.

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A. Use Case Diagrams

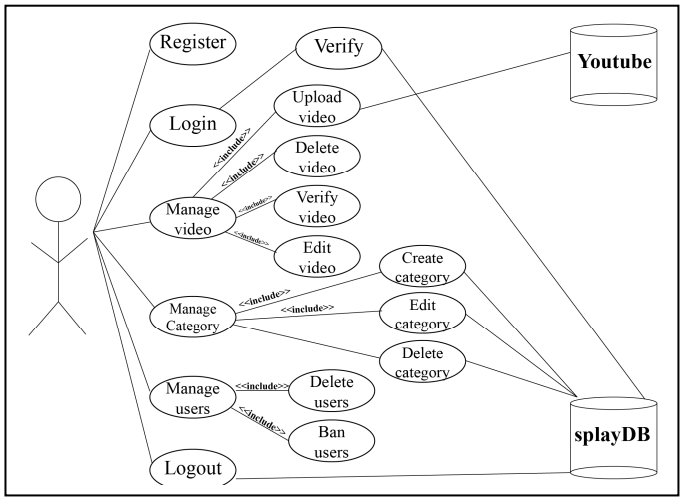

Fig 3.1 - Admin use case

Fig 3.1 enlightens the possible use cases of an actor, admin in the splay. As per the figure admin when interacts with splay, two more actors are in action. Splay uses its database when performing different operations such as managing users, videos, creating categories, managing sessions of admins/users, etc. The YouTube database is used while uploading videos.

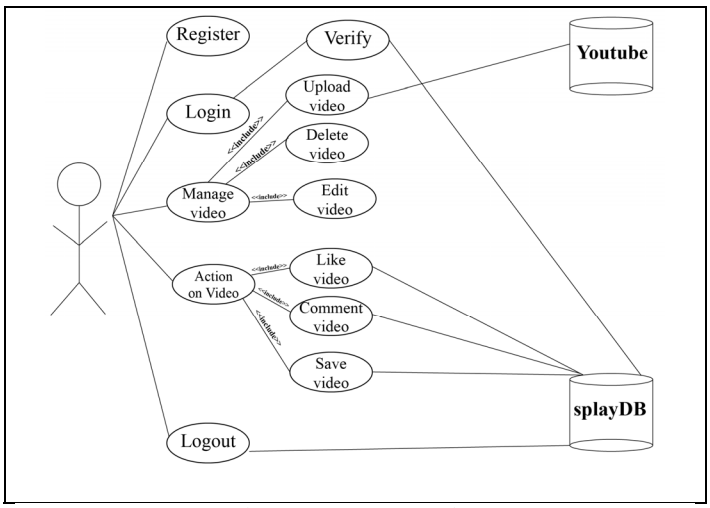

Fig 3.2- User use case Splay

The fig 3.2 also shows that the actor user interacts with two actor i.e. splay database and YouTube database. Users too have basic facilities like logging in and out of the application. They can manage their own video and like and comment on other videos. Users cannot manage other users in any way that power remains to administrator.

B. The Front End Part

The setup for react is created using the create-react-app tool chain provided by Facebook it and it is quite easy to get started with it. Just one command can set the entire environment you need for React. We'll be using npm (node package manager) for the packages and maintaining them in our environment. Command is as follows :

"npx create-react-app my-app"

Here, my-app will be the name of our directory. This command can also be initiated inside a particular folder by replacing the folder name with a dot or full stop(.). Splay uses third party libraries such as Material UI since it is based on Google's material design, react-router for making splay a single page application and react-redux for state management of components.

C. The Back End Part

We use npm for package management in the backend as well. On top of Node, we are using express, a lightweight node framework for faster development. For communication with the database, we use mongoose node package instead of the default available Mongodb drivers. Every route in the application which node serves is made a middleware for security of the routes. Users not logged in will be not be allowed to access some routes also any user should not be allowed to access admin's routes and hence routes are implemented as middleware's which act in the middle of the usual request and response process hence named middleware's. Splay is divided into three main directories namely models, routes and controllers. Models are mongodb models, routes are routes to each route application is going to serve and controllers are the functions to be performed by the servers when a particular route is requested.

IV. Mathematical Model

Mathematical modelling for streaming of videos in peer to peer network is done using the starting delay and buffer size. In the future times when organizations decide to conceal some of their content and make it visible to selected users or peer to peer video sessions, these mathematical model implementations will help. The model uses frames and chunks of videos and different delays to calculate the load. Splay can use its existing original servers for streaming of such video itself as following.

A. Starting Delay estimation

We denote the four types of delay in the mathematical model as follows: Start up delay as T_{std}, Playback delay as T_{pbd} , Starting delay as T_{stid}, delay T_d. The start-up delay is basically the time that user is supposed to wait until the first and foremost frame arrives in the buffer, playback delay is the time where user waits until the chunk in the buffer is filled, starting time is the total waiting time that user is supposed to wait until the first frame is displayed, delay is initial time according to the server time [9].

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1) Start-up Delay :

The start-up delay (T_{std}) depends on the number of neighbours used for content discovery and download. There are two scenarios -

a) One neighbor

T_{std} = Transmission delay + Tracker Time + Propagation delay + Peer Selection time + Exchange Buffer map time

$$T_{std}= \sum_{i=1}^{n} \frac{PacketSize}{TransmissionRate_i} + \sum_{i=1}^{n} (propagationDelay_i) + Trac\,\ker time + \sum_{j=1}^{L}\sum_{i=1}^{n} \frac{BufferMapPackageSize}{TransmissionRate_i} + PeerSelectionTime \quad (1)$$

(Assuming queuing delay and processing delay is negligible)
n denotes the number of link from sender to receiver denotes the number of peers present, Transmission Rate denotes the number of bits per second, Tracker time is the time to track all peers, Peer selection time is the time to download first chunk after selection of a peer, Exchange buffer map time is the time needed for a new comer to exchange buffers with peers present in the list [9].

b) More than one neighbour

In a case where more than one neighbour is present, it is obvious that there will be several paths. The first received frame will have the smallest delay. So let P_i be a path that is walked through nodes from a source to destination which means from i^{th} neighbour.

$$T_{stu} = \text{Min}\,(Delay_{P1}, Delay_{P2}, Delay_{P3\ldots} Delay_{Pk}) = \text{Min}\,(Delay_{Pi}) : I = 1,2,3,\ldots k \quad \ldots\ldots\ldots (2)$$

From Eq (1), Let's $Delay_{Pi} = T_{stu}$
K is the number of neighbours.
P_i is a denoted path from the i^{th} neighbour.

2) Starting Delay

The total delay for the first frame to be displayed is the starting delay (T_{stid}) . It relied on the join time, the start-up delay and the playback time. It can be calculated as :

$$T_{sti} = \text{Max}(T_{join}, T_{pbd}) + T_{stu} \quad \ldots\ldots\ldots (3)$$

B. Buffer Size Estimation

This can be estimated using the join time or the release time. The unit is seconds because the waiting time for displaying the video depends on the fill rate of the node. Delay might have a different effect if there are a few users and the user who joins late may not be able to view the whole stream. Here, the arrival condition is used and splay plans to implement such in its network. The arrival condition is :

$$\frac{N}{M} - T_{stud} \le T_{pbd} + T_{release} \quad (4)$$

N is the total number of chunks
M is the total number of nodes
T_{stu} is the waiting time until the first chunk arrives in the buffer.
T_{pbd} is the playback time
$T_{release}$ is the release time

C. Server Load

The server load can be calculated according to two different scenarios for non-clustering model. In the first one, all users join at the same time and start the video and in the second all users join using the arrival condition time, then all users will directly download video from server. Equation (5) is the worst case for non-clustering model since the server load is highest. The worst case scenario occurs when one peer joins over 25 chunks of the neighbour peer. Assuming the video has N chunks and N is divisible by 25, the maximum number of peers is N/25. So, the maximum number of chunks sent by server becomes, 25 Σ(1 + 2+ 3 +… M).

For the cluster model, there are two cases of : worst and best case. The worst case is that the server supports equal to maximum number of super nodes and the best case is that server supports only one super node, shown in equation (7) and (8) respectively [9].

Non-Clustering Worst Case :

$$SL_{NC} = \frac{25 \times M}{2}(M+1) \quad (5)$$

Non Clustering Best Case :

$$SL_{NC} = 1xN \quad (6)$$

Clustering Worst Case:

$$SL_C = SP\ x\ N \quad (7)$$

Clustering Best Case :

$$SL_C = 1\ x\ N \quad (8)$$

N is number of available chunks.

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V. Comparison and Analysis

Splay performs as a better solution to the content management problem of institutions desiring their own video streaming application. A complete package of ease to developers as well as users, it can be scaled and expanded in any way. Making it a Progressive Web App is just cherry on the cake. The power of PWAs can be seen in examples of the following implementations.

- *Treebo* launched a PWA and saw 4x increase in conversion rate over a year. Conversion rates for repeat users saw a 3x increase [10].
- Tinder cut load from 11.9 seconds to 4.69 seconds with their new PWA. The tinder PWA is almost 90% smaller than the native app [10].
- *BookMyShow's* PWA takes less than 3 seconds to load and has increased conversion rates over 80%. The PWA is 54x smaller than android and the 180x smaller than the iOS app [10].
- *Flipkart's* PWA is driving 50% of its new customer acquisition. Nearly 60% of the visitors to PWA have uninstalled the native app to save the space [10].

VI. Conclusion

With modern functionalities and modern technologies used, splay becomes a robust and trustworthy solution for small scale as well as large scale institutions and organizations for video streaming. Picking up good points from native as well as hybrid applications, splay stands between the two and provides better accessibility and more engaging experiences. Not only, client's device space splay also saves more than 90% of server storage as well as complex calculations by using YouTube for streaming videos. If the organization plans to upload their own content or provide peer to peer video streaming facilities, the provided mathematical model will be used. The technology stack used opens new opportunities for modern development and always widens the perspective for further scalability and updates.

References

[1] de Andrade P R M, Albuquerque A B, Frota O F, et al. Cross platform app: a comparative study[J]. arXiv preprint arXiv:1503.03511, 2015.

[2] Huy N P. Developing apps for mobile phones[C] Computing and Convergence Technology (ICCCT), 2012 7th International Conference on. IEEE, 2012: 907-912.

[3] Malavolta, "Beyond Native Apps: Web technologies to the rescue!", 2016 ACM.

[4] Andreas Biørn-Hansen, Tim A. Majchrzak and Tor-Morten Grønli1 "Progressive Web Apps: The Possible Web-native Unifier for Mobile Development", scitepress.org.

[5] A.Osmani, The App Shell Model. Accessed on Oct 15, 2019. [Online]. Available: https://developers.google.com/web/fundamentals/architecture/app-shell

[6] M.Gaunt, Service Workers : an Introduction. Accessed on Oct 15, 2019.[Online].Available: https://developers.google.com/web/fundamentals/primers/service-workers

[7] Official React Documentation, Accessed on Oct 15, 2019.[Online]. Available: https://reactjs.org/

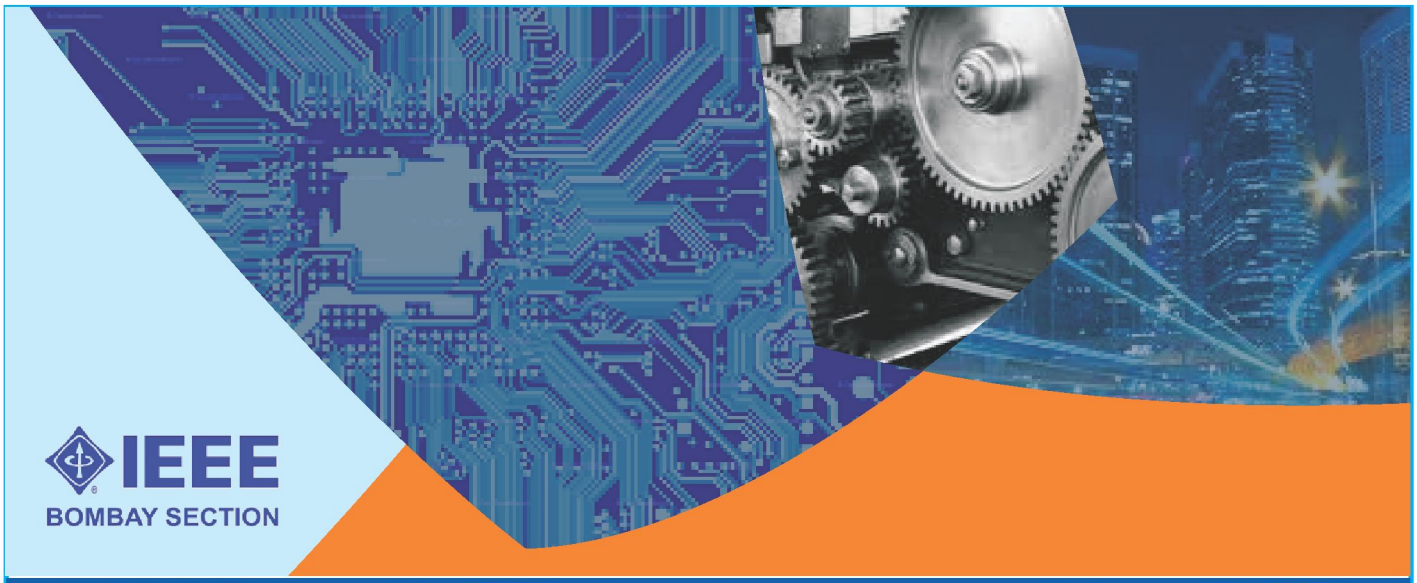
[8] Tilkov, S., & Vinoski, S. (2010). Node.js: Using JavaScript to Build High-Performance Network Programs. IEEE Internet Computing, 14(6), 80–83.

[9] H. Ketmaneechairat. P Oothongsap, A Mingkhwan (2012) Mathematical Models for different start video broadcasting. ResearchGate.

[10] PWA stats, Accessed on Oct 15, 2019 [Online]. Available : https://pwastats.com

Shri Sant Gajanan Maharaj Temple, Shegaon

Shri Sant Gajanan Maharaj College of Engineering, Shegaon
Khamgaon Road, SHEGAON Dist. Buldana (M.S.)



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Mahaganana: An Approach to a Smart Census in India

Jigar Wakhariya
Department of Information Technology
Student of Shri Sant Gajanan Maharaj College of Engineering
Shegaon, IN
jigarwakhariya@gmail.com

Prakhar Gangrade
Department of Information Technology
Student of Shri Sant Gajanan Maharaj College of Engineering
Shegaon, IN
prakhargangrade28@gmail.com

Amitkumar Manekar
Department of Information Technology
Faculty of Shri Sant Gajanan Maharaj College of Engineering
Shegaon, IN
asmanekar24@gmail.com

***Abstract*— In a large country like India where the population of states is equal to the population of other countries, it is very difficult to obtain the count of the population in a given minimum time and cost. Although the year 2021 is going to be the Census year for India, the 2021 Census is 8th Census (since independence) of country. In India, Census is conducted in every ten years by the government. This census is going to be very important due to many reasons. The previous censuses took place by the manual procedure that is very typical and is used since it has been introduced by the British in 1872. This procedure is very time consuming and requires large effort by mankind. So the need of the time is to simplify it. This could be simplified using technology. So we are using a Cross-Platform portal to conduct the entire process in a digital manner and introducing several changes in procedure of conduction of Census. This portal will serve to all. (i.e. Citizen, Census Officer, Ministers, etc.) and the entire procedure will be described as Mahaganana.**

Keywords—cross platform; census; cloud based census; machine learning;

I. INTRODUCTION

Due to the increasing population, the government is facing a problem of storing and maintaining the data of the Census by traditional methods i.e. by pen and paper, it is too time-consuming, and requires large human power. Around all this, a large amount of capital is also spent. So, there is a need to find a single solution for all these problems. The solution we want to propose is to change the existing Census system and to introduce a new system. This system will have certain phases that will minimize the time and cost required in the procedure. This system will convert the entire typical manual procedure into digital. This digital procedure will take place in 3 phases:

1) Registration Phase 2) Verification Phase 3) Grievance Phase

Before the Census, Government will initiate a campaign. They will make people aware of Mahaganana, the cross-platform portal, and registration on it. In the Registration Phase, the citizens can directly register for Census on the Cross-Platform Portal. This phase takes place at the Census Booth. Census Booths will be established by the government for a limited period in government offices, government schools, etc. Although the citizen can directly register by using his/her AADHAR ID on the cross-platform portal through their mobile/computers [1] but the biometrics record can only be done on the booth. So this will be citizen's choice to either perform registration and biometric record both on the booth or to only record biometric on the booth. The registration can be easier if AADHAAR ID is entered before registration, the data will be automatically updated and all other fields which are not pre-filled have to be filled by the citizen itself (like occupation, education, income, etc.) [2] on the cross-platform portal.

After filling the complete form and recording biometric the citizens will get notified that their information is recorded successfully. Then after some days, they will get pre-notification by SMS and Email regarding the schedule of visit of the officer at their home. They will also get basic details about the Officer along with their Photo. This will stop the frauds taking place by the name of Census Officers. This pre-notification regarding the visit of Officer will also stop the fraud of information stealing and its misuse. The information will reach to correct people only and such crimes can be stopped.

In the Verification phase, the census officer will visit each home (like previously done) and verify the information fed and documents. If the citizen wants to modify the filled data, the officer has the charge to do so only by checking the valid documents.

In the Grievance phase, the Census team will work on the data and find if any fault occurred and then perform required actions. For avoiding the problem of duplicate data, the data redundancies will be detected and removed by Normalization.

The time required for the entire procedure will be reduced as compared to the previous Census. As the registration will be done early, so the officer will need not

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register the citizens on the paper books and hence only verification will take place. It is not necessary for a citizen to compulsorily register by themself using their own Mobile/Computer, only the biometric verification has to be done by themselves at Census Booths only. The citizens specially handicaps who cannot reach the booth and have no access to the portal will be registered by the officers during verification. The registered citizen will get pre-notification regarding the visit of the officer at their home so they can reserve that time for Officer's visit [8].

As the primary key of the database will be AADHAR ID, the immigrant citizens staying illegally in India with fake AADHAAR ID can be easily detected. There will be no effect of weather on the Registration Process (as earlier, the government avoided to organize the registration phase during Monsoons in several high rainfall regions of the country).

II. METHODOLOGY

The workflow diagram for the working of procedure of the Census from the registration to verification is shown in fig 2.1. It is proposed as a modification to the standard procedure of 2011 Indian Census. The proposed idea is digital and has no role of pen and paper.

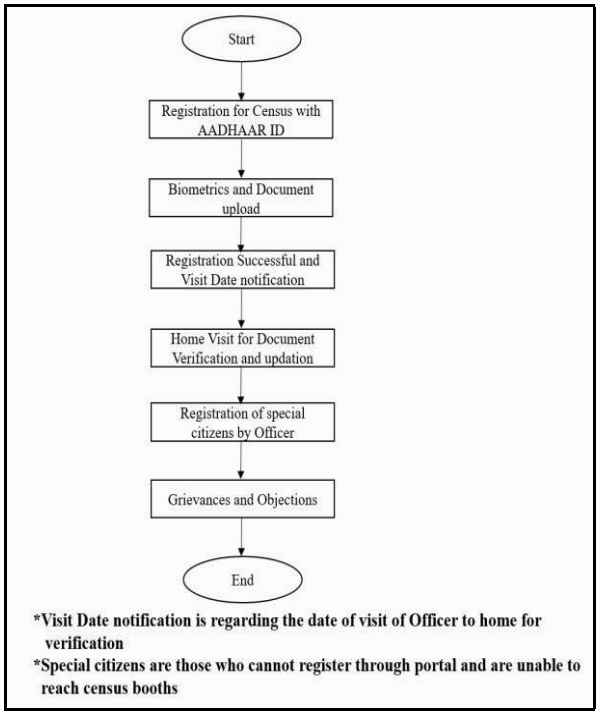

Fig 2.1 Workflow Diagram of Procedure

The procedure starts with registration of the citizen to the portal. This is the major step and thus does not allow the user to directly move to the next step. The registration is done by AADHAAR ID which will automatically fill the fields required in input and the other required fields are to be filled manually. The registration process can be done through mobiles and desktops or at the booth. The biometrics are very important and needed to be store/update. Although the biometrics information will directly come to the Census database when AADHAAR ID is registered. The biometrics are to be compulsorily recorded by each citizen. For this process, the citizen has to visit the booth. By completing this procedure the citizen will get a unique Family Id which can be used for registration of other members of family (this Id will remove several fields in the registration form). Along with Family Id, the citizen will get a message that registration is successful and a notification regarding the visit date of Census Officer to their home.

At the date of verification the officer will visit the home and verify the original document and the mentioned data in the registration phase. If there had been any mistake during registration or anything to be updated, officer is the only one who holds the authority to update this when they visit home. Along with this, the officers will also be responsible for the registration of Special citizens (those who cannot register through the portal and are unable to reach census booths). The officer will himself fill their registration form, record biometrics and will verify documents.

At last, the data will be compared, analyzed and operated using several algorithms, the redundancy will be removed and if any dummy entry or fake id detected then proper objections will be taken.

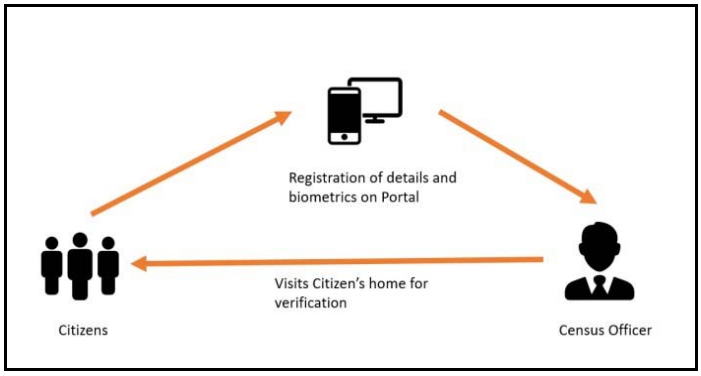

Fig 2.2 Sequence Diagram for entire Process

Fig 2.2 is the sequence diagram for the workflow of the entire process. This gives a brief description of relations between the actors. It states that the citizens register their data through mobile/desktop which will upload data at server/cloud which the census officer will access during the visit for verification. All this will be in function to IoT and will be real-time. So it is possible for Census Officer to register and verify quickly after that [3].

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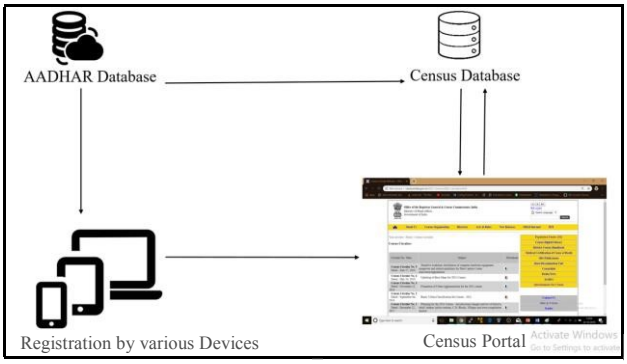

Fig 2.3 Sequence Diagram for flow of Data [6]

Fig 2.3 is the sequence diagram for the flow of data in between and throughout the databases. There are two databases: 1) AADHAAR Database, 2) Census Database. The user can register and input their data using mobile, computers, tablets etc. on the portal at the website of the Census of India. When the citizen enter their AADHAAR ID in the registration, the census database will fetch the data stored at AADHAAR Database.

The portal although will also be functional even after the census and it could be used for addition or removal of member present on a particular Family ID in case of Birth/Death by uploading appropriate Birth/Death Certificate. This Census data can be used for the next ten years for various analyses and predictions for various objectives by the smart predictive algorithms [4][5][7].

III. Mathematical Modeling For Biometric Census

Appendix I: Estimating the Annual Requirements of new UIDAI cards in terms of new Births by Gender and Region.

Let P(x) represent projected population of age x at time t, $s(x, x+1)$ is a survival function, which describes the chance of survival for an individual of age x to age $x+1$ and $F(x)$ is age specific rate of reproduction of new babies at age x. Then,

$$\sum_{x=18}^{50} S(x, x+1)P(x)F(x)K \quad \text{---- (1)}$$

Here equation (1), gives number of newly born babies that will be delivered by mothers aged between 18 and 50. Here, K is the proportion of eligible female out of total female in the reproductive age group.

Note: As per the law, the age limit for female marriage is minimum 18 years and age limit for female to adopt child is maximum 50 years of age [9][10].

Appendix II: Model for Estimating the Population Survived from Currently Living Population (a difference equation approach)

Using a simple difference equation, we can obtain the future survivors out of current living population. Suppose $P_r^{(t1)}(x, x+1)$ is the population available at census time point t1 and for region r for the ages $x = 0,1,2, \ldots \omega$ We can obtain the population who are surviving out of $P_r^{(t1)}(x, x+1)$ at the census time point $t2$ by using the survival function, $S_r^{(t2-t1)}(x, x+1)$, presenting the chance of survival of population of age x in a region r at census time $t1$ to live up to *age* $x+(t2-t1)$ at census time point $t2$. Such functions for all the ages can be computed if a life table is available for the region r. Thus, the population that survives throughout the time period $t2-t1$ and reaches the census time point $t2$ at age $x+(t2-t1)$,

i.e. $P_r^{(t2)}(x+(t2-t1), x+1+(t2-t1))$ can be expressed as, $Pr^{(t2)}(x+(t2-t1), x+1+(t2-t1)) = P_r^{(t1)}(x, x+1)S_r^{(t2-t1)}(x, x+1)$, for the values of x *0,1,2..., ω-1* For further information on difference equation models in biology see [9][10][11].

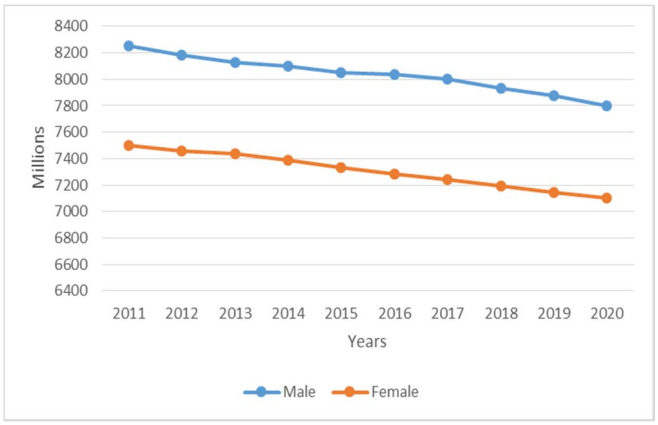

Fig 3.1 Predicted Annual Number of Cards Newly Required

Since the Indian population (provisional) for the year 2011 is 1,210 million (623 million males and 586 million females) [12]. In Figure 1, the number of male and female AADHAAR cards required per year after 2011 are shown in Fig 3.1. The Projected decadal population growth rate from the next Indian census i.e. 2011 to 2021 is 12.3 percent. Models can help to estimate the babies that will be born in each year by gender, by regions, by states in India in the near future with some degree of accuracy, which can be useful for planning and distribution of cards. (Mathematically proven in Appendix I & II).

IV. Conclusion

The 2021 Indian Census is definitely going to be digital all the way but the way it is going to take place and the ease it will provide to the citizens is not yet documented or disclosed yet. This is a proposed solution that will provide the maximum ease to the concerned authority and to the citizens too. This solution will lead to digital awareness among common citizens and a feeling of oneness and patriotism in

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common lives. This solution will also work on the redundancy of data, stopping malpractices and thefts taking place during the census and will work on accuracy more than the traditional systems.

REFERENCES

[1] Alessandro Lulli, Lorenzo Gabrielli et al. "Improving Population Estimation From Mobile Calls: a Clustering Approach", 2016 IEEE Symposium on Computers and Communication (ISCC)

[2] Sharath R et al. "Data Analytics to predict the Income and Economic Hierarchy on Census Data" 2016 International Conference on Computational Systems and Information Systems for Sustainable Solutions, pp.249-254

[3] Pavan Kumar, Haroon Sajjad, et al. "Analysis of Urban Population Dynamics based on Residential Buildings Volume in Six Provinces of Pakistan using Operational Linescan System Sensors" IEEE Sensors Journal, 2017, pp.1656 - 1662

[4] Syed Muhammad Sajjad Kabir, "Basic Guidelines for Research: An Introductory Approach for All Disciplines, Edition: First, Chapter: 9, Publisher: Book Zone Publication", Chittagong-4203, Bangladesh, pp.201-275, July 2016

[5] Bin Sheng, Sun Gengxin, "Data Mining in Census Data with CART", 2010 3rd International Conference on Advanced Computer Theory and Engineering (ICACTE)

[6] "Ministry of Home Affairs, Government of India" [Online]. Available: http://censusindia.gov.in/

[7] "2020 Census Research, Operational Plans", and Oversight. [Online]. Available: https://www.census.gov/programs-surveys/decennialcensus/2020-census.html#

[8] "The Challenge of America's First Online Census on June 2, 2019", [Online]. Available: https://www.wired.com/story/us-census-2020-goesdigital/

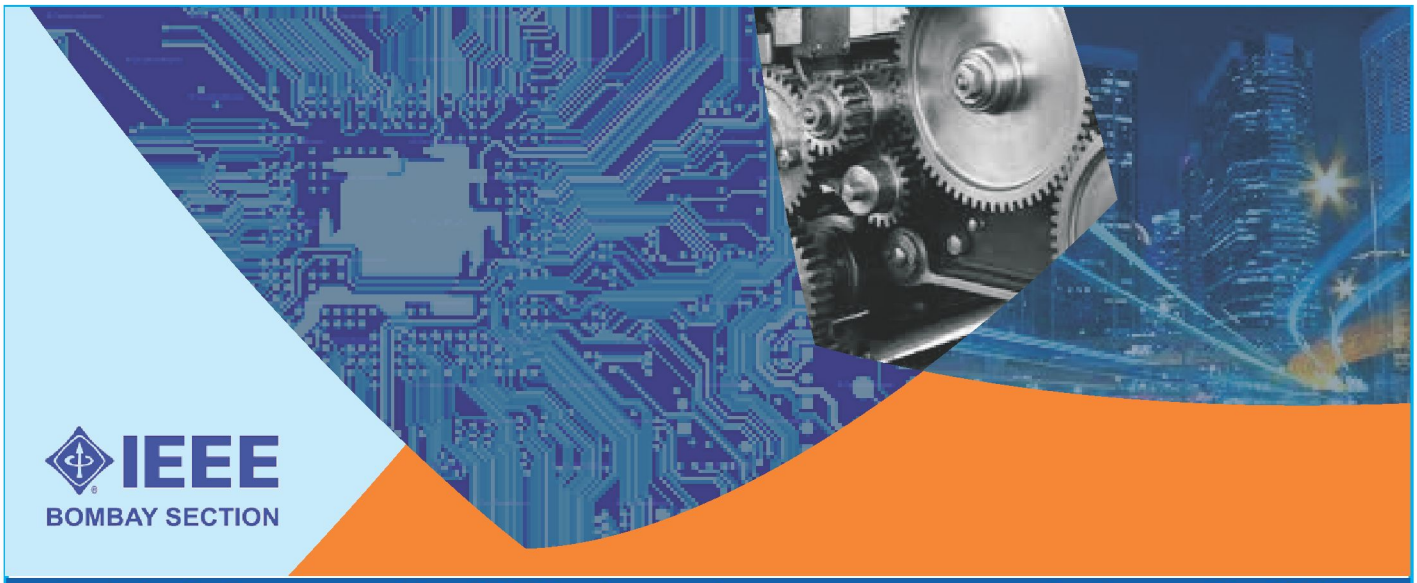
[9] Arni S.R. Srinivasa Rao "Biometric Cards for Indian Population: Role of Mathematical Models in Assisting and Planning" pp.1-8

[10] Murray, J. D. Mathematical biology. I. An introduction. Third edition. Interdisciplinary Applied Mathematics, 17. Springer-Verlag, New York, 2002.

[11] Keyfitz, N. "Introduction to the mathematics of population", Addison Wesley Publishing Co., London, 1968.

[12] "Provisional Population Tables and Annexures Census2011, Census of India, Govt. of India- Ministry of Home Affairs, India". [Online]. Available: (http://censusindia.gov.in/)

ISBN -978-1-7281-1901-4



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Optimize Neutral Framework With Fair Share Resource Allocator For Big Data Processing On Cloud Infrastructure

Amitkumar Manekar
Research Scholar, CSE Dept. KLEF,
Vaddeswaram, A. P. India.
asmanekar24@gmail.com

Dr. Pradeepini Gera
Professor, CSE Dept. KLEF,
Vaddeswaram, A. P. India.
pradeepini.gera@gmail.com

***Abstract*—Data is precious! Data generated from myriad resources are store and treated, extracted for getting knowledge through classical machine learning techniques. The MapReduce is a programming framework that proved its efficiency and reliability for big data processing in a distributed environment. When data are generated in a cloud platform the speed and volume of data are high. MapReduce has its own limitation over processing big data. Spark has also eliminated many boundaries especially dealing with online streaming and cloud generated data. Big Data cluster management is a tedious work that needs specialized algorithms for a fair share approach. Many time resource contention problems have to address with fair-share but the performance was not satisfactory. MESOS and YARN have an implementation of the same. The proposed framework use historical job execution logs for admission control and deadline information is an additional and important part which supplied at the time of submission of the job. The work anticipates different deadline formulation explained in the result section. Finally, a comparison of justice with existing fair share allocation policies is discussed.**

***Keywords—Resource-constrained; deadline; admission control; resource allocation; big data; cloud; spark; Genetic algorithms; Evolutionary Computation*.**

I. INTRODUCTION

Cloud computing already proved its importance in computational paradigms. Many industries are looking towards cloud computing as a prominent solution for future perspectives. Now with Fog computing and IoT one challenge is for utilization of cloud infrastructure for tomorrow's big data analytics is fair share resource utilization. To mitigate this issue massive BDA (data processing framework) namely Apache Spark is largest stake and accepted for local or cloud-deployed cluster processing for customized big data processing.

Spark framework works on a worker node with single or multiple available resources. This master node is in charge of the allocation of resources to distinguished applications. basically, resource allocation in spark is possible with the master node with 3 approaches. These three approaches are namely 1. Default Resource Allocation 2. Static Resource Allocation and finally 3. Dynamic Resource Allocation. The problem with these resource allocation single applications is running on default allocation strategies in clusters with all resource consumption rations. In static and dynamic user participation in resource allocation is mandatory. Hence severe performance issues are generated due to improper allocation of resources. If the production server mentions any default deadline the resource allocation will not work because with FIFO queue approach may force for an unnecessary wait. Discretization of data can be considered as optimization and minimal problem, evolutionary-based metaheuristic solutions are proposed widely [21]. With distributed solution having based on evolutionary heuristics could be [22] a problem for large scale big data processing. Gartner introduces big data [23] in 2001. Till its inception to the current date, many researchers contributed to efficient scalable time-efficient large scale data processing framework. Hadoop and MapReduce [24] are good enough for processing large scale data. The extremely popular approach of an open-source methodology of MapReduce is Apache Hadoop [25][26]. Hadoop and MapReduce both are not incepted for continuous streaming data and in-memory computation. On the other side Apache spark is faster than Hadoop (100X faster) with in-memory computations. Apache spark totally supported Read-Evaluate-Print Loop (REPL) approach dealing and processing large intensive data with data associated. Spark promoted linear MapReduce's linear scalability and fault tolerance, it focuses on 1. Broad directed acyclic graph (DAG) of operators by sending the result to the next step in the pipeline. 2. Richest set of conversions which effect to facilitate users to precise working out more unsurprisingly. 3. Spark works withs in-memory computing for a cluster of machines, it doesn't rely on storage space for transitional data in MapReduce. Apach

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Spark operation read and write from to NoSQL databases like HBase and Cassandra also it supports all read and write format which MapReduce Support.

Finally, we can conclude Apache Spark is sustaining large intensive scalable, high throughput, and fault-tolerant dealing out of living data streams. Live stream data is inputted and data streams during a receiver and segregates data into micro-batches, which are then processed by the Spark engine to generate the final stream of results in batches. This ultimately solves large scale distributed data streaming and data computation and processing problem. In the next section i.e. chapter II is a literature survey where we try to focus on current research and its paradigm's. Chapter III Optimization and Justice – Fair resource sharing chapter focus on the research gap and objectives of this work identified from chapter II i.e. literature survey. Finally, chapter IV is Experimental Setup and Methodology which focuses on Methodology for job tracking, Resource Estimation and Resource allocation 3 different algorithms where optimization was implemented by nature-inspired algorithms CAT Swarm algorithm for effective resource allocation. In the last section, a detailed discussion about the current scenario and proposed system performance are discussed.

II. LITERATURE REVIEW

For spark cluster manually resource allocation has to be done for application when tried to deploy on spark clusters, which ultimate limit the entire system to any parameters specified by users with constraints and minimize the cost of running applications. Apache Spark [1] is one of the most dominant big data processing platforms. Spark is open source basically and it's a widely adaptable large scale data processing framework with batch or stream data processing with machine learning or graph processing [2] capabilities with various distributed data sources like HDFS [2], HBase [3], Cassandra [4] etc. with Resilient Distributed Dataset (RDD) [5] for data abstraction. On the other side with in-memory computation spark has proven faster than MapReduce and Hadoop [6]. It express as a top module of Hadoop YARN [7], Apache MESOS[8] and the very important standalone cluster manager. Space sharing job schedulers [9] [10] to partition cluster resources for these platforms [11] [12] are not used by the cluster administrator. Existing BDA framework negotiate cluster manager accept resources and uses ultimately accepted resources [13].

In a broader perspective, each framework is aggregated with its constituent assembly mentioned as *1. Sharing on Multi-tenant Resource Allocators 2. Performance Prediction 3. Admission Control [14] [15].* Combinable all these assembly work for efficient performance. an SLA deadline is given for job finishing and guaranteed that the service usage cost is reduced are focused [16][17] but in a limited way. We focus on time-sensitive Spark framework which generally used industry for e-commerce applications [18], web search platforms[19], web content hosting and live video streaming like Netflix[20]. For Optimization, many nature-inspired and prominent algorithms such as Genetic Algorithm (GA)[27][28], Ant Colony Optimization (ACO) [29], Particle Swarm Optimization (PSO) [30], and Simulated Annealing (SA) [31] are proposed and checked in different segments of framework. Data aggregation's with OLM (online lazy migration algorithms) and RFHC Randomized Fixed Horizontal Control are proposed by Linquan Zhang et. al. [32].

III. OPTIMIZATION AND FAIR RESOURCE SHARING POLICY

Big Data Analytics (BDA) is processed for discovering hidden values from large data using parallel processing and infrastructure. Facebook, eBay like BDA applications needed optimized search result which use massively high-performance computing power. On the other side, large data storage with an on-demand approach is needed. Although together with increasing benefits of cloud computing has inevitable challenges. QoS (Quality of Service) with invariant services are the major bottleneck for cloud computing infrastructure. To address all the challenges the number of researchers invented and suggested various solutions. To the optimized quality of BDA applications in the cloud such as performance, reliability, and security. Some of the research work such as G-Hadoop is fine-grained data processing frameworks that leverage MapReduce. All tenants in cloud computing are charged based on VM occupation. Hard Bandwidth Guarantee and Minimum bandwidth guarantee is provided in perceptive to performance in cloud computing.

IV. PROPOSED METHODOLOGY NEUTRAL FRAMEWORK

In this work, we proposed a Neutral Framework which actually interfaces between tenants and providers for cloud computing with deadline requirements. All BDA jobs required large cloud computing jobs such as forecast analysis, social media, and e-commerce. The worst part of these jobs is a deadline if the job finishes after the deadline result will be useless. There must be a provision that cloud resource allocation will be as per deadline awareness before sharing the resources.

Proposed algorithms need open source operating systems like Linux environment. With second generation of 4 Intel

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processor having 8 GB of RAM. As platform implementation will be on JAVA and python.

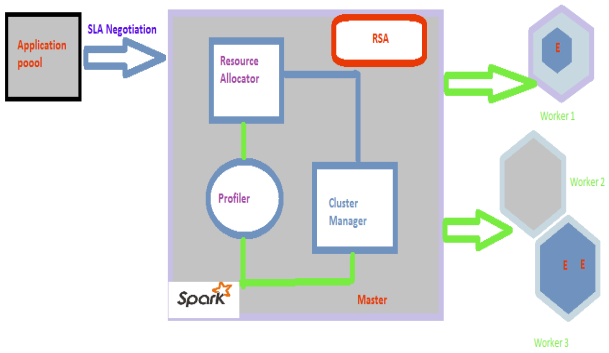

Fig: 4.1 Spark Based Deadline Framework.

As shown in figure 4.1 clouds provider offered tenants the flexibility of resource allocation for meeting the deadline for computing a job. This framework required to advertise deadline as well as a resource needed (No. of VM's bandwidth for each VM's and time duration) from each tenant to cloud provider. Now resource allocation algorithms work superiorly for allocation of resources by computing deadline for reach job and a fraction of resources available.

Problem Formulation: - in this section discuss a formulation of FRAS- fair resource allocation system based on Apache Spark with a deadline is to discuss and algorithms for executions are discussed.

A. Optimal cost resource allocation approach –

In apache-spark master and worker nodes are being deployed on cloud VM's (virtual machines). Assume that these Virtual machines (VM's) are homogenously used In extension assumption is made about all virtual machines that have the same computation power, i.e. same CPU(cores), storage and computational memory. Now for fair share resource allocator (FSRA), Resource allocator (RAS) must advertise CPU cores, storage, and computing memory. Table 4.1 mentions some notations used for fair share policy formation. Our ultimate goal is to keep optimal fair share resource allocation.

TABLE 4.1 NOTATION AND PARAMETER

Symbol/Notation	Definition
Asp	*Application deployed on cloud*
E_X	Executors
P_{tvm}	Price of VM's (per Second)
M	Memory
C	CPU cores w.r.t executors
R_E	Price of executors
W_n	*Workers*
W_c	Worker core
W_m	Worker Memory
E_{max}	Max Possible execution
t_c	Completion time of any application
D_p	Deadline parameters

B. Algorithm- FRAS-Fair resource allocation system based on Apache Spark-

For the execution of algorithm an application to be submitted to Spark Cluster with desired RSA w.r.t possible resources computing like (CPU), Memory (M), and total executors(E_x) per application. The algorithm mentioned specified FRAS- fair resource allocation system based on Apache Spark. Prior knowledge of the total resource amount of cluster need is essential.

Algorithm-FRAS-*Fair resource allocation system based on Apache Spark*

Initiation of A_{sp}
Advertise D_p, P_{tvm}
Calculate (M) where $f(C(W_c * W_m))$
Calculate E_{max} *where* $f N (W_c * F))$
Compute ***FSRA***
If $E_x = E_{max}$
    Execute ***FSRA***
        else
        $FSRA <- \{ C, M, E_x \}$
        $FRSA <- RSA + FSRA$
        $E <- E+1$
Execute ***FSRA***

An algorithm is executed with Spark API called as Spark Launcher API build in JAVA after submitting an application to the cluster. The total numbers of worker nodes are homogenous in nature. At the initiation configuration of one worker node is given. After calculating M and E_{max} values algorithms $_a$ total number of executors may vary. And in step 7 of algorithms RSA is calculated and added to the FSRA scheme.

If splitting or partitioning of input then it will be an overhead on actual processing or running time. If the numbers input chunk exceeds with respect to actual executors then this chunk must be processed as a batch. The algorithm will outperform the only resource that will not be wasted. Therefore for a fixed input SLA requirements are 100%

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satisfied. Deadline based resource allocation and spark combination are used with application scheduling.

V. RESULT AND DISCUSSION

We have proven many promising features of cloud computing with a fair resource sharing facility and deadline scheme. As a result finally, we are able to discuss possible solutions and limitations. There are some grand challenges *1) Job Scheduling*- jobs scheduling with laxity. Job scheduling is a parameter for interpretation between time (to run) and resources available i.e. VM's completely depends on parallelism of job. *2) Pricing – The* proposed model presumes that deadlines are very much clear to the user before proceeding to job execution. *3) Learning* – Our framework significantly learned many things from observation. Most of the time framework observed time series sequence can be used to the prediction of the future. *4) Robustness*-practically to run efficiently framework need robustness. Robustness should be accountable in both planned and unexpected failures in any dimension. Majorly resource failure is a big challenged to achieve robustness. Ultimately QoS needs to be the focus. MESOS and YARN use fairness criteria, whereas suggested method estimate fraction of request resource effectively just before finishing the task with deadline expire time. Perhaps making this estimate when the job is entered for processing using the requested number of resources as the number necessary to complete the job as early as possible. Each big data analytic framework calculates the expansion factor is computed and tally across jobs, fair share resource allocation is possible. An exact evaluation of workload implementation of these two algorithms is targeted in JAVA, as a majority of frameworks support JAVA platform. For computing expansion factor is computed across jobs a script issued for implementation extended Kalman filter is used. Extended Kalman filter correct inaccuracies of its initial estimations.

Both MESOS and YARN the resources allocator will be use by job to it indentify and with no limit on the turn-around time a job's owner is willing to tolerate. Proposed algorithms we basically focus on partial local knowledge of job submitted along with trade-off between the statistical data from remote clouds and cloudlets that each cloudlet process and store locally with respective the amount of information exchanged within the distributed. "Risk" for running frequent jobs with available resource may be with high or fewer than it they consume so that it can adapt its allocations automatically to changing workload parameters need to consider while implementing for robustness.

VI. CONCLUSION

In this paper designed to Optimize Neutral framework with fair share resource allocator for extensive big data processing on cloud infrastructure are proposed. The novelty of this framework is it meets deadlines and job execution efficiently. In first insight, a user needs to specify resource required and a deadline to complete the job need to advertise. Our framework efficiently utilized resource request most appropriately. Extensive experiments should be conducted to compare baseline allocation and recently proposed VM allocation, neutrally framework finishes more jobs, make better utilization of VM's and network resources which sustainably achieve QoS and gain much more revenue for a service provider. We assured about comparison of different fair share schedulers and an Oracle using multiple deadline strategies: a fixed multiple (Fixed), a random multiple (Jockey), a uniform multiple (Aria) of the actual computation time, and mixed loose and strict deadlines (90loose) in near future [33]. Assuming in resource constrained clusters, when CPU demands exceed available cluster resources, fair-share mechanisms can violate fairness.

Proposed methodology is also aware that adding ability simply drops jobs which tend to missed their respective deadlines does not improve the fairness in resource sharing completely. Proposed system may not be useful when large jobs are meeting their deadlines and finish jobs before deadline. Proposed algorithms are best performing on open source resource management platforms like MESOS and YARN. Constrained IoT analytics settings are firmly needed some optimize solutions for big data processing. Proposed algorithms take care of Optimizing resources and investigate parameter for supervision that would require larger number of computing resources which is nothing but additional overheads without adding any kind of complexity with minimal information from resource manager and user. As future work, we are planning to extend the proposed algorithms on live job track record generated by YARN and MESOS so it can deal with more diverse workloads. Considering infeasible deadline cluster cannot satisfy the deadline suggested by user in ideal condition allocation by providing incentives to user. We also try for minimizing and adaption of FRAS for replication and repetition of jobs. Last but not least, just like all these investigate approaches, proposed algorithm gives priority and strongly recommend on processing job with satisfaction job deadlines in addition to preserve fair-sharing across jobs utilize the cluster.

REFERENCES

[1] M. Zaharia, T. Das,et.al. "Apache spark: A unified engine for big data processing," in Communications of the ACM, 2016.

ISBN -978-1-7281-1901-4

[2] K. Shvachko, et .al. "The hadoop distributed file system," in Proceedings of the 26th IEEE Symposium on Mass Storage Systems and Technologies (MSST), Washington, DC, USA, 2010.

[3] L. George in HBase: the definitive guide: random access to your planetsize data. " O'Reilly Media, Inc.", 2011.

[4] P. Malik and A. Lakshman "Cassandra: a decentralized structured storage system," ACM SIGOPS OS Review, 2010.

[5] M. Zaharia et. al., "Resilient distributed datasets: A fault-tolerant abstraction for in-memory cluster computing," in Proceedings of the 9th USENIX Conference on Networked Systems Design and Implementation, San Jose, CA, 2012.

[6] S. Ghemawatand J. Dean, "Mapreduce: simplified data processing on large clusters," Communications of the ACM, 2008.

[7] V. K. Vavilapalli, et al., "Apache hadoop YARN : Yet another resource negotiator," in Proceedings of the 4th ACM Annual Symposium on Cloud Computing, Santa Clara, California, 2013.

[8] B. Hindman, et. al. "Mesos: A platform for fine-grained resource sharing in the data center." in Proceedings of the 8th USENIX Conference on Networked Systems Design and Implementation, Boston, MA, USA, 2011.

[9] V. Misra,et. al., PBS: a unified prioritybased scheduler. In: ACM SIGMETRICS Performance Evaluation Review. Vol. 35. 1. ACM. 2007, pp. 203–214.

[10] Pradeepini, G. et. al., 2017. "Opportunity and Challenges for Migrating Big Data Analytics in Cloud", IOP Conference Series: Materials Science and Engineering 2017

[11] GERA, P. et. al, 2016. "A recent study of emerging tools and technologies boosting big data analytics"

[12] M. A. Jette, et. al., Slurm: Simple linux utility for resource management. In: Workshop on Job Scheduling Strategies for Parallel Processing. Springer. 2003, pp. 44–60.

[13] https://hadoop.apache.org/docs/r2.4.1/hadoop-YARN /hadoop-YARN site/FairScheduler.html. for YARN Fair Scheduler.

[14] B. Hindman et al. Mesos: A Platform for Fine-Grained Resource Sharing in the Data Center. In: NSDI. 2011, pp. 22–22.

[15] M. Hu et al. Deadline-Oriented Task Scheduling for MapReduce Environments. In: International Conference on Algorithms and Architectures for Parallel Processing. Springer. 2015, pp. 359–372.

[16] T. Chestna, S. Imai, et. al. , "Accurate resource prediction for hybrid IAAS clouds using workload-tailored elastic compute units," ser. UCC '13.

[17] G. Singer, et. al., in "Towards a model for cloud computing cost estimation with reserved instances," CloudComp 2010.

[18] Pradeepini.G., et. al., "Cloud Based Big Data Analytics a Review" , Proceedings - 2015 International Conference on Computational Intelligence and Communication Networks, CICN IEEE 2016, pp. 785-788

[19] W. Golab, et. al. in "OptEx: Deadline-Aware Cost Optimization for Spark," Available at https://github.com/ssidhanta/ OptEx/blob/master/optex_technical.pdf, Tech. Rep., 01 2018.

[20] "Netflix at spark+ai summit 2018," by F. Siddiqi, in 2018.

[21] N. Xiong, et. al., "A walk into metaheuristics for engineering optimization: principles, methods and recent trends" , International, J. Comput. Intell. Syst. 8 (2015) 606–636.

[22] S. Cheng, et. al., "Evolutionary computation and big data: Key challenges and future directions", in: Proceedings of the Data Mining and Big Data, First International Conference, DMBD 2016, Bali, Indonesia, June 25–30, 2016, pp. 3–14.

[23] D. Laney, et. al., in 3D Data Management: Controlling Data Volume, Velocity and Variety, 2001.

[24] S. Ghemawat,et. al., "MapReduce: simplified data processing on large clusters", in: Proceedings of the 6th Conference on Symposium on Opearting Systems Design & Implementation, vol. 6 of OSDI'04, 2004, pp. 10–10.

[25] Pradeepini. G. , et. al., in "Experimenting cloud infrastructure for tomorrows big data analytics", International Journal of Innovative Technology and Exploring Engineering, 8(5), pp. 885-890.

[26] Apache Hadoop, 2016. (Online; Accessed December 2016). http://hadoop.apache.org- in Apache Hadoop Project.

[27] Goldberg,et. al., in "Genetic Algorithm in Search. Optimization and Machine Learning". Addison Wesley Publishing Company (1989).

[28] F. R., Jack, et. al., in "Application of Parallel Genetic Algorithm and Property of Multiple Global Optima to VQ Codevector Index Assignmen". Electronics Letter 32(4) (1996) 296-297.

[29] R., Kennedy and Eberhart, in "A new optimizer using particle swarm theory". Sixth International Symposium on Micro Machine and Human Science (1995) 39-43.

[30] Roddick, Chu, et. al., in "Ant colony system with communication strategies", Information Sciences 167 (2004) 63-76

[31] Pan, J. S., et. al., in "Vector quantization based on generic simulated annealing", Signal Processing 81(7) (2001) 1513-1523

[32] L. Zhang, et. al , " Moving Big Data to cloud : An online cost-minimization Approach," IEEE Journal on selected areas in communications , vol. 31, no. 12, pp. 2710-2721, 2013.

[33] Stratos Dimopoulos, Chandra Krintz et.al. "Justice: A Deadline-aware, Fair-share Resource Allocator for Implementing Multi-analytics", 2017 IEEE International Conference on Cluster Computing (CLUSTER), PP-233-244.

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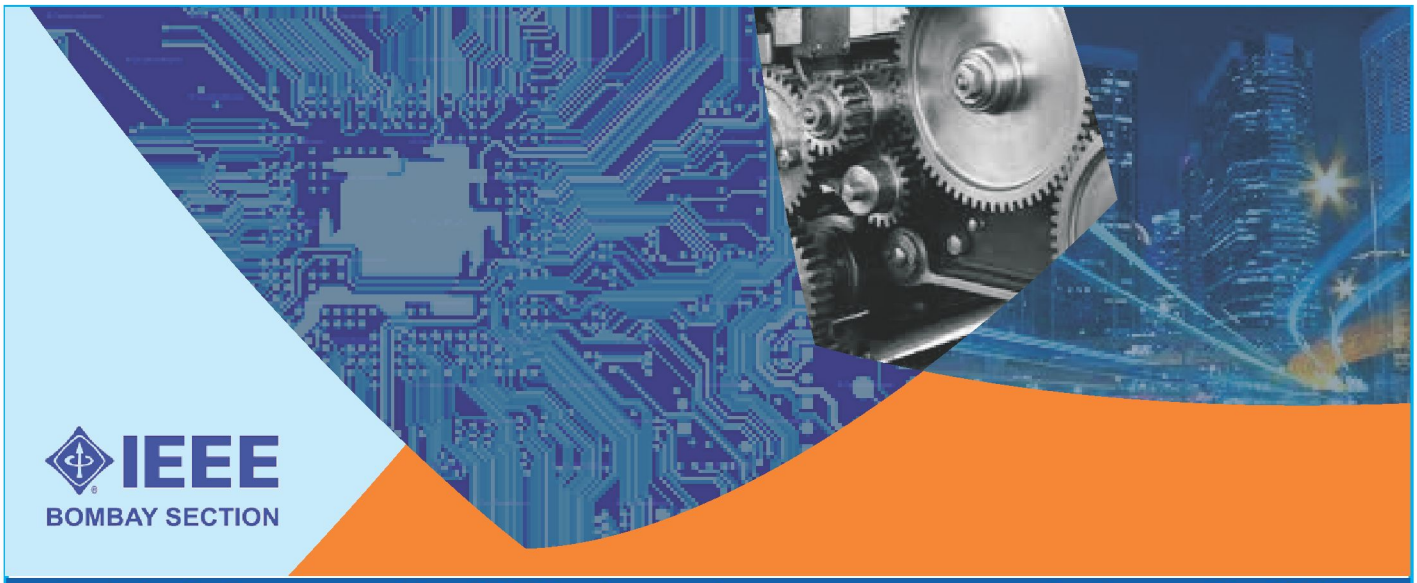
Shri Sant Gajanan Maharaj College of Engineering, Shegaon
Khamgaon Road, SHEGAON Dist. Buldana (M.S.)



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An Effective Data Hiding Mechanism Based on Encrypted Images

Aniket K. Shahade
Assistant Professor
SSGMCE, Shegaon

Priyanka V. Deshmukh
Assistant Professor
SSGMCE, Shegaon

Dr. A. S. Kapse
Assistant Professor & Head
AEC, Chikhali

Dr. V. M. Thakare
Head, Dept. of CSE
SGBAU, Amravati

***Abstract*— Now a day's to stay up secrecy associated confidentiality of an data can be a vibrant field with two completely different approaches being followed, the first being encrypting the images through cryptography algorithms victimization keys, the other approach involves concealing information victimization information concealing algorithmic rule to stay up the images secrecy. A content owner use cryptography key to perform the cryptography of original footage, and using a data concealing key an information hider can plant any data into the encrypted image though he does not acknowledge the primary content, as a result of the encrypted image contains some any data, with the help of cryptography key a receiver first decipher it then extract the embedded data and recover the primary image in line with the data-hiding key.**

Keywords— Cowl image, Knowledge concealing, Knowledge extraction, Image secret writing, Image decoding, Knowledge recovery, DWT.

I. INTRODUCTION

Cryptography is a method for securing the key information that we tend to transferring from one purpose to a special. In cryptography sender encrypts the message exploitation the key so sends it to the receiver. Once receiving from the sender the receiver decrypts the message to urge the key data. The main focus of encrypting the data i.e cryptography is to keep the content secret so that the information concentrates on keeping the existence of the secret message [3]. To establish a secured communication the other technique is information Security. Information security involves security of information so it appears like no information is hidden within the smallest degree. Somebody views the message that's hidden within he or she is getting to haven not got any construct that there is any hidden data, so as that it's really hard for person attempt to decipher the information [4]. Information security of image has many applications, notably in today's trendy, sophisticated scenario. Privacy of data and secrecy of data could also be a priority for several people in the network. Hidden image allows for two parties to talk secretly or covertly. The strength of data activity gets amplified if it combines with the cryptography. In information activity, the terminologies used area unit cover-image, hidden image, secret message, and secret key and embedding algorithm.

Cover-image is that the carrier of the message likes audio file, video or image. Cover- image carrying the embedded secret information is that the hidden image. Secret message is that the knowledge that's to be hidden throughout a cowl image. The key secret might be a clothed plants the message depending on the activity algorithm [4]. The embedding algorithm is that the design , that's utilized to plant the key information at intervals the duvet image. The securities of the transformation of hidden information square measure typically obtained by two ways: Cryptography and knowledge activity. Mixes of the 2 technique square measure typically accustomed increase the knowledge security. Cryptography could even be method throughout that the message is modified in such how so as that no information square measure typically disclosed if it's received by associate wrong actor. Whereas in information activity, the key message is embedded into a picture sometimes mentioned as cowl image, so sent to the receiver agency extracts the key message from the quilt message. Once the key message is embedded into cowl image then it's mentioned as a hidden image [8]. The visibility of this image shouldn't be distinguishable from the quilt image, so as that for offender it nearly becomes insufferable to look out any embedded message. Here, we've a bent to work the info concealment technique that's reversible in nature. So it's termed as Reversible data concealing-technique.

In severable reversible data concealing technique, firstly a content owner encrypts the first uncompressed image [1], then associate data hider compress the image to make house to accommodate some any data. Reversible data concealment are often a way to linear measure graft any message into some distortion-unacceptable cowl media like military or medical footage with a reversible manner in order that the primary cowl content is totally restored once extraction of the hidden message.

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II. LITERATURE REVIEW

Fridrich et al. (2001) [5], planned the reversible information embedding technique for the authentication purpose that the embedding capability of this technique is low. Zhang empty out house for knowledge embedding within the plan of press encrypted pictures, to filter the data extraction from image cryptography [6], [7]. An encrypted binary image could even be compressed with a lossless manner by finding the syndromes of low-density parity-check codes, a lossless compression technique for encrypted grey image victimization progressive decomposition and rate compatible cut turbo codes is developed in [6]. W. Liu, W. Zeng, the loss compression technique given in [7]. An encrypted gray image could even be efficiently compressed by discarding the excessively rough and fine information of coefficients generated from orthogonal transform. A receiver might reconstruct the principal content of original image by retrieving the values of coefficients, once we get the compressed knowledge. The computation of transform among the encrypted domain has additionally been studied X.Zhang[8].

W. Liu, W. Zeng planned, once we transmit the encrypted secret knowledge, a channel supplier with none data of the cryptanalytic key might tend to compress the encrypted knowledge due to the restricted channel resource, a lossless compression technique for encrypted image victimization progressive decompose and rate compatible turbo codes is developed in [7]. the tactic in [8] compressed the encrypted LSBs to vacate house for other information by finding syndromes of a parity-check matrix, and thus the info that's employed at the receiver facet is that the special correlation of decrypted image. RDH (reversible data hiding) in plain domain aims at developing a way that increases the embedding capacity as high as possible while keeping the distortion as low as possible. Since we consider RDH in encrypted image, the embedding capacity is comparatively more important, and therefore the concern over image quality degradation caused by data hiding are often alleviated or maybe neglected [1]. a completely unique method by reserving room before encryption with a standard RDH algorithm, and thus it's easy for the info hider to reversibly embed data within the encrypted image. The proposed method are able to do real reversibility, that is, data extraction and image recovery are freed from any error. All previous methods embed data by reversibly vacating room from the encrypted images, which can be subject to some errors on data extraction and/or image restoration [2].

III. ANALYSIS OF PROBLEM

Now a day, a fresh challenge consists to insert knowledge in encrypted pictures, because the entropy of encrypted image is largest, the embedding step like noise isn't potential by victimization common place knowledge concealing algorithms. New plan is to use reversible knowledge concealing algorithms on encrypted pictures by desire to urge obviate the embedded knowledge before the image cryptography. there's one another downside if either concealing key or cryptography key's leaked then welcome person will extract or rewrite the image through data concealing key or rewrite the image through cryptography key.

Another downside found is that, the key use for encrypting the image and knowledge concealing is same. That the user who is conscious of the key use for cryptography will access the embedded knowledge and original knowledge. We are ready to retrieve the primary image from encrypted image when extraction or removing the data hidden within the image. The content owner and knowledge hider share constant cryptography key for cryptography of image and knowledge concealing. Up to the present , there's no provision of choosing the key and extra encoded code time consumption. there's various knowledge concealing programs on the market. variety are glorious in each respect sadly, several of them lack usable interfaces, or contain several bugs, or inconvenience of a program for alternative operative systems.

IV. PRAPOSED WORK

Data concealing provides simple approach of implementing the strategies. the foremost purpose behind this is often often to provide a economical technique for concealing the data from hackers and sent to the destination firmly. this system is principally involved the formula ensuring the secure knowledge transfer between the availability and destination. For that we tend to initial used cryptography then knowledge concealing and vice-versa. In knowledge concealing we'll use cowl image for security purpose. The medium during which info is to be hidden is termed as cowl image. The key use for encrypting the image and knowledge concealing is same. To resolve that drawback we'll use one secret key for encrypting the image and another secret key for knowledge concealing. A content owner encrypts the primary image victimization cryptography key and employing a knowledge-hiding key a data-hider will plant further data into the encrypted image. With an encrypted image containing further knowledge, receiver might initial decode it keep with the cryptography key, then recover the primary image keep with the knowledge hiding key by extracting the embedded data. Thus, if the each keys square measure completely different then there are a unit sample securities in knowledge transmission.

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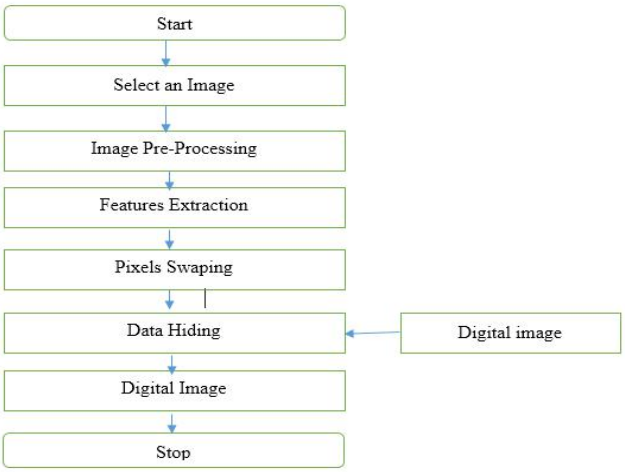

Fig.1. Data Embedding Flowchart

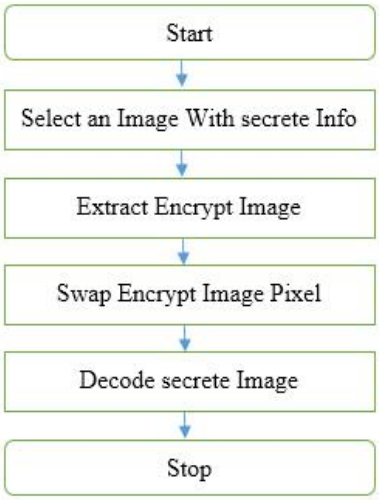

Fig.2. Proposed Data Extraction Flowchart

V. THE PROPOSED ALGORITHMS

A. Feature Extraction Process:

This section 1st describes the feature extraction module that extracts feature pictures from the natural shares. The module which is that the core module of the feature extraction method is applicable to written and digital pictures at the same time. Then, the image preparation and also the pixel-swapping modules are introduced for process written pictures. Assume that the scale of the natural shares and also the secret image area unit w nine h pixels which every natural share is split into variety of b nine, b picture element blocks before feature extraction starts. We tend to outline the notations as follows:

1. b represents the block size.
2. n denotes natural shares.
3. x, y denotes coordinates of pixels in the natural shares and secret image x1.w, y1.h
4. x1,y1 represents coordinates of left top pixel in each block.
5. Φ denotes the value of color code like R,G,B.
6. Pixel value $H_{x,y}$ is the sum of RGB color value of pixel x,y.

B. The Image Preparation and Pixel Swapping Processes :

The image preparation and pixel swapping processes are used for preprocessing written pictures and for post processing the feature matrices that are extracted from the written pictures. The written pictures were handpicked for sharing secret pictures, but the contents of the written pictures should be non heritable by computational devices so be reworked into digital data. The advised flow of the image preparation method is shown in Fig. 3. Within the initiative, the contents of the written pictures are often non heritable by well-liked electronic devices. To reduce the excellence within the content of the non heritable pictures between the encoding and cryptography processes, the type of the acquisition devices and therefore the parameter settings (e.g. resolution, image size) of the devices need to be constant or similar in each processes. subsequent step is to crop the extra pictures. Finally, the images are resize so as that they need constant dimensions because the natural shares. An example of the image preparation method is illustrated in Fig. 4.

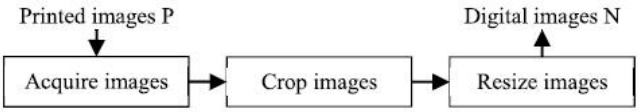

Fig. 3. Flow of the image preparation process

Fig. 4. Example of image preparation method : (a) A hand printed image (b)The resultant picture

C. *Encryption/Decryption Algorithms:*

The planned theme will code a true color secret image by n-1 innocuous natural shares and one noise like

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share. For one image, we tend to denote a trifle with an equivalent weighted price within the same color as a trifle plane, then a real color secret image has twenty four bit planes. Thus, the feature pictures and therefore the noise-like share are also extended to twenty four bit planes. Every plane bit of a feature image consists of a binary feature matrix that corresponds to an equivalent bit plane because the secret image. Before cryptography of every bit plane of the key image, the planned algorithmic program initial extracts n-1 feature matrices from n-1 natural shares. Then the bit-plane of the key image like noise share and n-1 feature matrices execute the XOR operation to get the bit plane of the share image. Therefore, to cipher a true color secret image, the cryptography procedure should be performed iteratively on the twenty four bit-planes.

VI. CONCLUSION

Here during this paper, planned an honest technique of data concealing in an exceedingly separate ripple zone of carrier image. It contains most utilization of data and conjointly pictures in an exceedingly single carrier image. At the time of decipherment if any of images is corrupted then we'll rewrite alternative pictures in same carrier image. It contains maximum utilization of channels and since of this we will hide maximum data at a time.

VII. RESULT

A. *Input Printed Image*

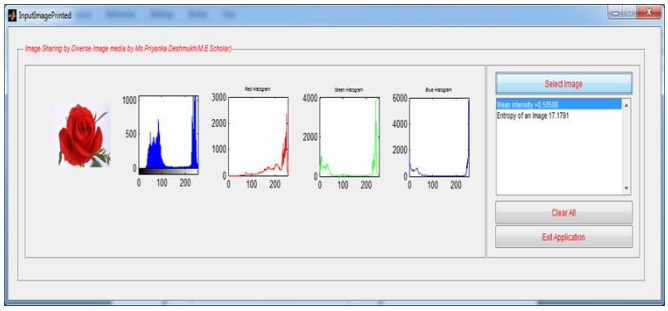

Fig.5. Input Printed Image

B. *Input Digital Image*

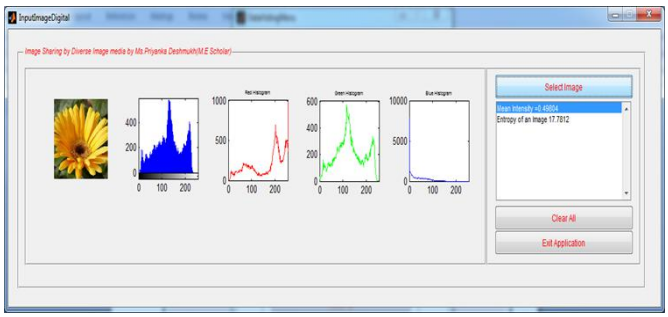

Fig.5. Input Digital Image

After performing all operations on printed image, the resultant extracted original image is:

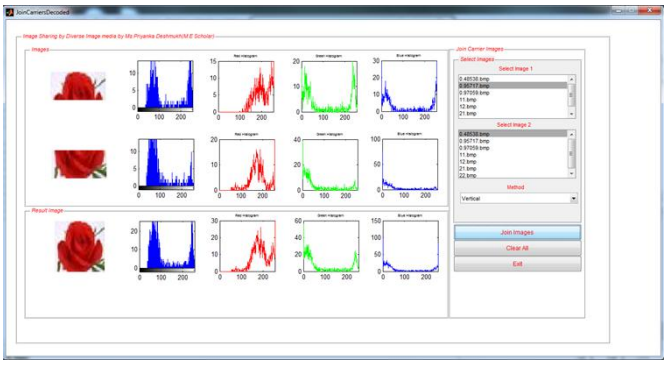

Fig.7. Extracted Original Printed Image

C. *Comparison between original Printed image and extracted printed image with respect to Entropy:*

TABLE I. COMPARISON WITH RESPECT TO ENTROPY

Sr. No.	Printed Image	Entropy of Printed Image	Entropy of Recovered Printed Image
1.	Red.jpg	17.1791	17.486
2.	Girl.jpg	17.5022	17.7035
3.	Rose.jpg	17.9348	17.885
4.	Violet.jpg	17.3617	17.1862

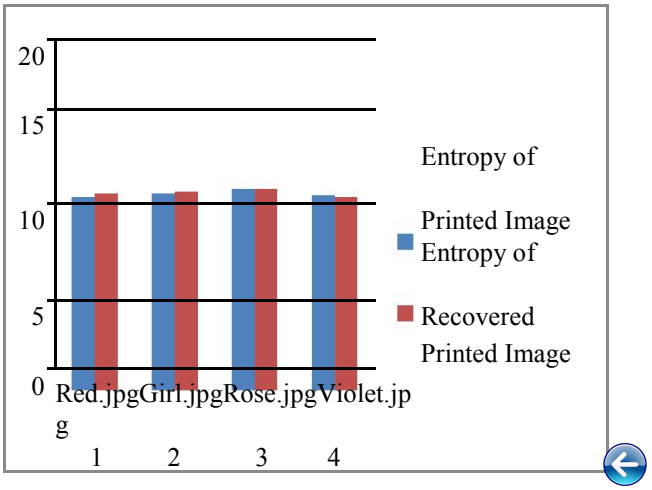

Fig.8. Entropy Graph

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REFERENCES

[1] F. Huang, J. Huang, and Y. Q. Shi, "New framework for re-versible data hiding in encrypted domain". IEEE Transactions on Information Forensics and Security, vol. 11, no. 12, pp. 2777-2789, 2016.

[2] K. Ma, W. Zhang, X. Zhao, et al. "Reversible data hiding in encrypted images by reserving room before encryption," IEEE Transactions on Information Forensics Security, vol. 8, no. 3, pp. 553-562, 2013

[3] Lini Abraham, Neenu Daniel ," Secure Image Encryption Algorithms: A Review", International Journal of Scientific & Technology Research volume 2, issue 4, April 2013, PP-186 189.

[4] Mohanraj Arumugam and Rabindra Kumar Singh,"Data Hiding and Extraction Using a Novel Reversible Method for Encrypted Image" IJREAT International Journal of Research in Engineering & Advanced Technology, Volume 1, Issue 1, March, 2013, PP-1-5.

[5] Kim, H.J., Sachnev, V., Shi, Y.Q., Nam, J., Choo, H.G. 2008. A novel difference expansion transform for reversible data embedding. IEEE Transaction Information Forensics and Security 3 (3), 456–465.

[6] M. Johnson, P. Ishwar, V. M. Prabhakaran, D. Schonberg, and K. Ramchandran, "On compressing encrypted data," IEEE Trans. SignalProcess., vol. 52, no. 10, pp. 2992–3006,Oct. 2004.

[7] W. Liu, W. Zeng, L. Dong, and Q. Yao, "Efficient compression of encrypted grayscale images," IEEE Trans. Image Process., vol. 19, no. 4, pp. 1097–1102, Apr. 2010.

[8] X. Zhang, "Separable reversible data hiding in encrypted image," IEEE Trans. Inf. Forensics Security, vol. 7, no. 2, pp. 826–832, Apr. 2012.

[9] X. Zhang, "Reversible data hiding in encrypted images," IEEE Signal Process. Lett., vol. 18, no. 4, pp. 255–258, Apr. 2011.

[10] X. Zhang, "Lossy compression and iterative reconstruction for encrypted image," IEEE Trans. Inform. Forensics Security, vol. 6, no. 1,pp. 53–58, Feb. 2011.

[11] W. Puech" Image Encryption and Compression for Medical Image Security" PROCEEDING OF IEEE Image Processing Theory, Tools & Applications.

[12] W. Puech, M. Chaumont and O. Strauss "A Reversible Data Hiding Method for Encrypted Images" Author manuscript, published in "IS&T/SPIE Electronic Imaging 2008 - Security, Forensics, Steganography, and Watermarking of Multimedia Contents, San Jose, CA : United States".

[13] Jiang Yu, Zhenxing Qian, "Reversible Visible Watermark Embedded In Encrypted Domain", 2015

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IoT and BLE Beacons: Demand, Challenges, Requirements, and Research Opportunities-Planning-Strategy

Sagar D. Padiya
SGBAU, Amravati,
Maharashtra, India
padiyasagar@gmail.com

Dr. Vijay S. Gulhane
Sipna COET, SGBAU
Amravati, Maharashtra, India
vijaygulhane27@gmail.com

Abstract - The Internet of Things (IoT) has various technologies that improve the functionalities of IoT devices to make them capable to connect and communicate with each other. The IoT with various advanced technologies and devices performing a rapid transformation of current society towards easier and smarter. As the use of IoT increases, the new challenges, requirements, and research/ innovation need have arisen to fulfill the demands. Wireless devices with low power and high data security are the most viable demand for diverse IoT applications. In an IoT environment, various nodes/ sensors are used to collect the data and different wireless communication technologies like Infrared, Bluetooth, Li-Fi, WI-Fi, Zigbee, etc. are used to transceive the data. As per the survey, among all other available wireless technologies, Bluetooth Low Energy (BLE) beacons have proved as most promising short-range wireless communication technology due to the fact of appearing everywhere or of being very common of Bluetooth-compatible technology. However, for better performance and efficiency of BLE beacons in the IoT ecosystem, regular research has needed to ensure seamless integration. For such research here we have combined the literature of IoT with Beacons. This paper consolidates: an introduction of IoT with its current market demand, challenges and five essential requirements observed. We have also discussed the research planning and strategy to discover the solutions. It also consolidates an introduction of BLE Beacon with its market demand, a survey of existing/ proposed solutions are reviewed to identify the current problem statements for research opportunities in the future.

Keywords – Internet of Things; Wireless Communication; Bluetooth Low Energy; BLE Beacons

I. INTRODUCTION TO IOT

In the Internet of Things (IoT) environment, each device has a connection with all other devices connected in the same network so that they can communicate with each other. Now a day, many IoT systems involve smart sensor networks, which have mainly connected by a wireless communication medium, generally known as a Wireless Sensor Network (WSN) [1]. Due to small size and limited computational power, nodes of such networks are called, ‘motes'. Motes can also directly connect to the Internet to integrate the web servers. The facility of motes interaction with web servers allows for creating a web of sensors called Web of Things (WoT) [2].

In our personal lives, smart IoT devices are becoming ever more prevalent and pervasive. Due to the IoT era, sensors are everywhere in smart society, and the trend will continue in the future. Today, industrial equipment with sensors in Robotic Process Automation (RPA) have powered by advanced technologies like artificial intelligence (AI), machine learning (ML), cloud computing (CC), etc. In the last decade, the IoT importance has notably improved up to 15.4 billion IoT devices installed in 2015 which is targeted to 30.7 billion in 2020 and 75.4 billion in 2025 [3]. In the magazine "The Five Essential IoT Requirements and How to Achieve Them-2019", Cognizant observed that enterprises that adopted IoT have decreased supply chain costs by more than 20%, increased productivity by 10% to 20% and reduced design-to-market times by 20% to 50%. [4]

The day-to-day nature of IoT applications becoming more complex as it includes, the number of functionalities with heavy databases and advance technologies. To manage and configure a plethora of IoT devices, large numbers of protocols are required. For a broad range of applications, higher levels of protocols are required. However, as the number of protocols in the IoT system increases, the increase in the deficiencies of product quality occurred. To improve the quality of IoT, a deeper understanding of these protocols in sense of their security, configuration options, and the application requirements are required for proper design and development of the best protocol.

II. CHALLENGES OF IOT

[4] In the "The Five Essential IoT Requirements and How to Achieve Them-2019", Cognizant observed that as seek to reap the benefits of IoT, enterprises are facing many challenges, including selecting, implementing, customizing and supporting new technologies across the IoT continuum, from sensors and cloud platforms to analytics and AI, understanding and implementing unfamiliar data formats and proprietary communication protocols, and integrating the IoT infrastructure with existing systems without overloading corporate networks, compromising security, exceeding budget or falling behind competitive efforts.

III. REQUIREMENTS OF IOT

The above challenges require careful planning, domain knowledge, and rigorous implementation. [4] Based on work with clients, Cognizant researchers have identified the following five essential requirements for processes and practices that should be part of every IoT implementation. In this survey, we are considering the following requirements for research in the future by the scholars.

1) Edge computing/analytics:

In the IoT system, edge computing involves the computation and analysis of data on distributed devices positioned at the edge of a network system. It involves both local sensors that gather data and edge gateways that process it. The notable advantage of an edge-computing architecture is that data can be analyzed close to where it is captured, resulting in a faster response to changing conditions. Additionally, edge gateways can transform proprietary or legacy protocols into IoT protocols for transmission to existing corporate networks or the cloud.

Gateways and sensors operate in the low-bandwidth condition at the network edge. In addition to perform edge analytics, the gateways can also pre-process and filter data to reduce transmission, processing and storage costs, as well as send commands to IoT devices and perform software upgrades. Data needs to be gathered by sensors and analyses in real-time to

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provide rapid response to sudden change. An edge-processing system can respond earlier compared with a cloud system.

Research Planning and Strategy:

i) To perform edge computing and analysis firstly assess the lifetime device and maintenance costs, Also assess the operational overhead expenses for device-monitoring, device-up-gradation, and power-requirement. These parameters are important to adjust planning so that such costs do not outweigh lifetime value.

ii) Design the policies for the security of devices by applying appropriate firewall systems. Wherever necessary use model system security systems like digital signatures, encryption algorithms, authentication systems, etc.

iii) IoT devices have a limitation of power so always perform the data aggregation to avoid repeated data transmission over the network. Always perform transmission of aggregated data with proper encoding format and packet size. For critical data transmission whenever necessary use separate frequencies.

iv) To detect and prevent failures during data sharing with external systems use the retry and circuit breaker patterns.

v) Perform the application at the edge to allow immediate action as per the assessment and analysis of the application.

2) Data ingestion and stream processing:

In IoT system data ingestion refers to devise telemetry in which data is imported and converted into a format usable by cloud-based IoT services. Processes need to be in place for gathering data from multiple devices/ sensors and transforming it for use by cloud-based analytics platforms. 60 % of researchers agreed that collection, storage, integration and analysis of the real-time data from end-point devices is a major barrier for the successful implementation of the IoT system.

Research Planning and Strategy:

i) To apply data ingestion and stream processing firstly assess the expected data size, criticality and expected system response time to select the cloud components to fulfill the requirement.

ii) As per assessed data size, perform data telemetry on a dedicated, higher-bandwidth channel. The use of bandwidth as per assessment reduces the bandwidth and related costs.

iii) Apply cache frequently-needed data to avoid repetition from the source, this will improve the performance while reduces network cost.

iv) To perform protocol conversion, configure the gateway and hardware with high computing and storage capacity.

v) To achieve consistent and high-performance data ingestion use load balancing, horizontal auto-scaling, and failover data processing systems

3) Device management:

In the IoT system, device management involves the hardware, software, and processes to maintain and ensures devices are properly registered, managed, secured and upgraded. It also has the notification system in case of device failure."

Required functions include device-configuration, security, command-dispatching, operational-control, remote-monitoring, and troubleshooting. The organization will need to account for these functions, even if the cloud provider does not offer the required device management components. Comprehensive device management enables connected devices to easily and securely communicate with other devices and cloud platforms while helping the enterprise reliably scale to billions of connected devices and trillions of messages. Businesses need to ensure their IoT devices have provisioned securely, communicate efficiently and can be updated with accelerated and agile approaches that result in energy efficiency. Device management should reliably scale to billions of connected devices and trillions of messages.

Research Planning and Strategy:

i) For device management firstly always create dedicated channels and processes for various types of device data so that proper use of available bandwidth to increase scalability. For sensor-data businesses maintain separate approaches for data files

ii) In a system use of the dedicated, persistent, bi-directional channel to transmit device commands improves reliability.

The system must provide facilities for quick addition of new devices to the network, auto-registration through validation with a trusted system, etc.

iii) The device management helps to reduce management costs by applying an abstraction layer for greater automation of processes.

iv) Whenever necessary use a content delivery network to reduces the delivery time for device software updates.

4) Cold path and advanced analytics:

In the IoT system, cold path processing performs the analysis of large amounts of data by advanced algorithms after the data is stored on the cloud platform. Deep dives into IoT data should result in cost savings, as well as insights to create new products and new revenue models. Processing at large scale includes loads greater than 100K events per second or that have a total aggregate event payload size of over 100MBPS.

Research Planning and Strategy:

i) To perform cold path and advanced analytics in the IoT environment firstly drive the most insights from data by combining data from multiple sources through a complex processing framework. By inferring meaning from complex situations, dynamically define and process the analytical rules.

ii) Perform the data storing in its native format to consolidate data for easier access.

iii) To achieve high data accessing speed, categorize telemetry data by message size and the receiving application's needs.

5) Enterprise integration with business systems:

IoT system integration with business applications and enterprise systems make enables the sharing of raw and processed data, as well as analysis-driven insights. With deep enterprise integration, the IoT architecture can deliver benefits such as improved efficiencies, reduced costs, increased sales, heightened customer satisfaction and the ability to create and lead the new markets. To share data and insights businesses need mechanisms such as application programming interface (API) gateways, service buses, and custom connectors.

Research Planning and Strategy:

i) In enterprise integration applications, firstly evaluate communication needs such as simple message broker, request/response and data-level integration, data volumes, performance requirements and the integration needs of downstream systems.

ii) Provide self-service APIs to develop an ecosystem that enables integrators and developers to consume data and business insights.

iii) Whenever necessary use RESTful APIs to fulfill on-demand data sharing in various formats and among disparate systems.

iv) Design a high data-ingestion queue system on the cloud to pass large volumes of data.

IV. INTRODUCTION TO BLE

As the name introduces Bluetooth Low Energy also known as Bluetooth LE, Bluetooth Smart, or BLE is a wireless communication technology designed to achieve secured and energy-efficient data transmission than the classic Bluetooth. Due to the low power requirement, the BLE allows small devices to operate on tiny batteries.

In 2001, Nokia had realized a need for low power consuming wireless technology and published its solution after three years, named Bluetooth Low-End Extension. The design and development of BLE began in the first half of 2001. It had appealed to develop a device to perform secure data transmission and as small as possible in size. In 2006, Nokia had launched a wireless technology that would run alongside Bluetooth, known as

Wibree [5]. It had operated on very little power, but it had performed transferring of data three times slower. After negotiations with the Bluetooth Special Interest Group (Bluetooth SIG), it had decided to include, Wibree in futures Bluetooth specifications, as Bluetooth ultra-low-power technology, which we know today as BLE [5]. The low power latency nature and lower complexity structure make BLE perfect to perform at low-cost microcontrollers. BLE is a radio standard design with the lowest possible power consumption, specifically optimized for low cost, low bandwidth, low power, and low complexity.

After reviewed all other available wireless technologies for communication, we have decided to focus on BLE, which becomes an ultimate technology for many IoT applications due to the following main reasons:

• BLE has embedded massively in the latest smartphones.
• It is supported by the iOS, Android, Linux, OSX, Windows and all other main operating systems.
• It is capable to run as per IPv6 [6].

The research on BLE is a continuing process, which results in progressive improvement. For instance, to Bluetooth 4.2, Bluetooth 5 increases the network from 50 meters to 200 meters with a doubled speed [7].

V. INTRODUCTION TO BLE BEACON

BLE Beacon is a small-sized 32-bits ARM Cortex M0 CPU configured by 2.4 GHz radiofrequency using Bluetooth 4.0 Smart. Bluetooth SIG maintains various versions of Bluetooth smart devices. As per the meaning of the beacon, we can consider it a small lighthouse. Only in beacon instead of light has radio signals and instead of ships, it alerts to the observer about its presence. SIG claims that Beacons are capable to broadcast up to a range of 70 meters (230 feet). As per our reviews, due to the effect of noise in real-world conditions, practically users experienced a range of about 40 - 50 meters.

BLE configured smart devices can detect the broadcasted frequency signal and calculate the distance by measuring received signals strength (RSS). The signal strength depends on the distance. The beacon does not broadcast continuously - it broadcast frequency periodically called advertising. In setting users can set the period value called Advertise Time. As less advertising, the more frequent the broadcasting, the more reliable the signal detection. BLE does not require pairing; a phone can detect and executes multiple beacons at a time. BLE beacons are small devices which periodically broadcasts specific data packets to show its presence or to transmit certain information. Beacons are generally useful for indoor navigation systems and indoor positioning systems.

In the latest forecast, ABI research predicted the annual Bluetooth devices shipment to reach 5 billion up to 2021. At this time only smartphones have a share of 43% of total shipments. BLE shows the highest notable growth with a predicted 34% CAGR (Compound Annual Growth Rate) between 2016 and 2021, driven by new opportunities in beacons. As a result, Bluetooth smart devices will contribute 27% of total Bluetooth shipments by 2021 [8].

VI. SURVEY OF EXISTING FEATURES OF BLE BEACONS

Although the foundation of protocol and hardware developments of BLE beacons to implement IoT applications and services have a strong nature. Beacon already has many advantages like small-size, lightweight-data-transmission, low-cost, low-maintenance, and less-energy-consumption but also it has limitations in terms of broadcasting-range, storage-capacity, battery-capacity, and other hardware resources [9]. Due to its inherent architecture and broadcasting with pairing nature, the beacon has some drawbacks like large fluctuation in RSS, finite battery capacity and data security. Such weaknesses make beacon infrastructure difficult to implement and manage in trusted systems.

To solve the above mention drawbacks up to a certain level the development of BLE beacon involves the benefits of the big data and advanced signal-processing techniques. The BLE beacon infrastructure performs distance estimation, battery measurement & monitoring, security features, and scalable-server architecture & algorithms. In this section, the current state of development has reviewed and discussed in detail [10].

A. Battery Monitoring:

After deployment of the beacon infrastructure, the battery status monitoring to perform the replacement of battery on time is pre-requisite. As per the advertising packet specification, the battery voltage level has set inside the TLM frame of the Eddystone protocol. When any observer detects the broadcasted frequency, it can get the battery information along with an advertising packet [10].

To validate the accuracy of the battery-monitoring-system, a practical experiment has conducted. To achieve the above objective in experiment comparison of the measured battery voltage level and the actual battery voltage level is done which demonstrated that the battery-monitoring-system is sufficient to provide the approximate battery life status to a user [10].

B. Distance Estimation:

Distance estimation is the main technology for many IoT applications. The RSS is a cost-efficient method used for distance computation, but the result of RSS is not accurate always, the reliability of the final estimation result has errors due to fluctuation. Many researchers already suggested that the distance estimation accuracy can be improved by first obtaining a reliable RSS measurement.

[11] F. Yin, et. al introduced an RSS threshold optimization method to improve RSS for estimating distance for indoor applications. [12] N. Patwari and A. O. H. III performed the experiment and concluded that the error rate of the distance measurement is even higher than the RSS measurement. Therefore for developing IoT applications, accurate distance information is very important. [13] X. Shen, et. al published the traditional centroid localization algorithm which claims a significant accuracy improvement by 63%. In the presented algorithm beacon's position is calculated by measuring three intersecting points of beacons' regions. [14] A. Thaljaoui, et. al presented a different approach to calculating a path loss index by comparing the RSS at 1m and the target distance.

C. Security Features:

Due to beacon's simplistic broadcasting architecture, it is prooved as an extremely scalable system, the broadcasted data can be easily detected, hacked, abused or used by any other unauthorized user. Such attacks included but are not limited to physical attacks, such as thievery and vandalism, but also cyber-attacks and sabotaging such as device spoofing, beacon hijacking, piggybacking, Denial of services, packet injection, battery drainage attack, and selective frequency jamming.

Beacon spoofing permits beacon services outside its service area also; in some applications, such as the scavenger hunt at CES 2014 [15] and 2016 [16], beacon spoofing is undesired. The packet injection method is very similar to beacon spoofing, instead of placing a cloned beacon outside the service area, it has placed within the original network, disturbing its normal operation.

In the case of local area services, such an attack may lead to a critical system malfunction. [17] P. Misra illustrated the potential damage of this type of attack. [18] C. Kolias demonstrated the battery drainage attack on a single beacon, rendering it inoperable.

To secure beacon infrastructure, day-to-day many solutions have been proposing, for example, geo-location validation and cloud-based token authentication. In the geo-location validation

approach, geo-location detail of every beacon has pre-registered on an online server. GPS module broadcast location details with beacon signals to the server, thereby ensuring the physical presence of the broadcaster beacon near the observer. This approach helps to secure the beacon infrastructure from spoofing attacks [5]. However, such security systems have many loopholes. 1) The pre-registration of each beacon's geo-location detail on an online server is complex and resource-consuming, which reduces the scalability. 2) Geo-location validation would be possible only in outdoor because of the limitation that the GPS readings in indoor environments are unreliable, [5].

In the cloud-based token authentication, method beacons adopted a method to generate a beacon unique identification based on a token value. The generated token value can consider as a true UID for beacon and can only be deciphered by the cloud server. However, this UID generation method has implemented at the firmware level of the device, i.e. once the algorithm generated UID is discovered by the attacker, the system can be abuse so such a framework is difficult to deploy onto an already existing infrastructure [5].

D. System Scalability:

Beacons are devices used for the application of interaction between beacons and the edges (e.g., smartphones, smart wearable, etc). Beacons are generally used to measure RSS and estimate distance; they also involve network requests made to corresponding cloud servers. Therefore, to optimize the loading and improve the performance for beacon applications, the study of server scalability is necessary.

After ranging a new beacon, the edge sends the detected UID to servers using HTTP requests. For example, in a shop user can get product information when close to the respective beacon(s) [19].

VII. RESEARCH OPPORTUNITIES OF BLE BEACON

After a long study/ inspection of BLE beacon, we can trust on the feasibility and suitability for IoT applications. The flexibility, low-cost hardware and ease of deployment characteristics by BLE protocol allow a great degree of freedom for developers and make the infrastructure more affordable and scalable. However, it has observed that there are still some drawbacks, such as limited battery life, lack of interoperability between different BLE profiles, weak security and so on. In this section, to overcome the above drawbacks following some opportunities of BLE beacons have discussed and future research directions have suggested.

01. Research Opportunity: Beacon must support both protocols (iBeacon and Eddystone) simultaneously:

BLE detector protocols support only to the same type of protocol at a time. There are two frames are available for iBeacon and Eddystone. The protocol datagram is varied with each other. Some developers designed beacons to support both protocols, but practically, it can only support one protocol at a time. Developers or users need to perform switching between the protocols manually. While most developers incorporate such a switching system to facilitate both protocols, the switching has to be performed during the development or configuration phase. Once the beacon has deployed with a particular protocol, it is very hard to change the protocol mode [20].

Now a day, no beacons design available in the market that supports both protocols running simultaneously. We consider the above problem as a research opportunity i.e. to work and propose a design for BLE beacon which will support both protocols simultaneously.

02. Research Opportunity: Beacon must perform many-to-many interactions:

In the IoT era, many-to-many interactions within the same given region along with the deployment of multiple beacons required. However, in an environment with dense beacon deployment, interference is an issue affecting smooth and interruption-free interaction. In such an environment, beacons may interfere with one another only if they are closely spaced [0].

We consider the above problem as a research opportunity i.e. to work and propose a design for BLE beacon, which will allow many-to-many interaction in the network.

03. Research Opportunity: Energy Efficiency of BLE Beacon:

Opportunity is in the field of wireless sensor networks although energy-harvesting devices have well studied. Energy harvesting for BLE is useful in an outdoor environment only. For the indoor environment, it is not perfectly useful, a study is required for energy harvesting in indoor environments. Due to such limitations of energy harvesting in an indoor environment, IoT devices usually require lightweight data transmission protocols that optimize the use of resources and energy consumption.

We consider the above problem as a research opportunity i.e. to work and propose a design for lightweight protocols in the different layers of the IoT stack. The lightweight data transmission approach extends device battery life while degrades latency i.e. achieve guaranteeing Quality of Service (QoS). The lightweight protocol approach broadcast only small size data hence minimizes communications, computational load and storage need into the beacon. The use of standard protocols in the current IoT system provides system scalability, interoperability, and functionality. Therefore, such lightweight protocols have to be:

- Compatibility with every other already existing protocol
- Flexibility to implement into beacons, wearable or more robust gateways
- Scalability to support its applications in a newly upgraded platform.

04. Research Opportunity: Better Distance Estimation:

As per the reviewed studies, due to the instability of BLE signals, it is very difficult to achieve accurate distance estimation. The closest signal sources can be identified easily, as the signal sources were not closed to each other, unlike in a beacon infrastructure. Hence, an inaccurate RSS measuring creates problems to estimate beacons distance. The fluctuation in RSS value is a new challenge in developing beacon related applications. In the future, the RSS measurement needs to stabilize to avoid c fluctuation in distance values. [5]

We consider the above problem as a research opportunity i.e. to work and propose a design for BLE beacon, which will achieve a better accuracy assumption as a beacon's RSS will vary for different devices.

VIII. CONCLUSION

The IoT with advance technologies and supporting devices have a huge potential to transform society. IoT with wireless connectivity, BLE beacons play an essential part in realizing this new paradigm. To recognize the potential of IoT and BLE beacons, in this paper different aspects of IoT and BLE beacons are studied. In the first half, the introduction of IoT with its market growth/ demand, Challenges, and Requirements have discussed based on the survey of Cognizant Digital - 2019. For all derived requirements, we have also suggested research guidelines. The research scholar can take help from suggested research planning and strategy to find the solution quickly.

In the second half, the introduction of BLE Beacon with its market growth/ market demand, various challenges to identify research opportunities have studied. In this paper, we have observed the various research opportunities to improve the BLE beacon's performance. The research opportunities are respect to the system and software for BLE beacons. For the same, the connection in the network, battery performance, distance estimation, data security features, and server scalability were surveyed in-depth.

REFERENCES

[1] Ariel M Campoverde M., Dixys L Hernández R., and Bertha E Mazón O., “Cloud computing con herramientas open-source para Internet de las cosas” in MASKANA, CEDIA 2015.

[2] Dominique D. Guinard and Vlad M. Trifa, “Using the Web to Build the IoT”, in Manning Publications: April-2016.

[3] Sam Lucero, “IoT Platforms: enabling the Internet of Things”, whitepaper IHS Technology, March-2016.

[4] "The Five Essential IoT Requirements and How to Achieve Them" whitepaper by Cognizant Digital Business in February 2019.

[5] Christian Alexander Goosen, "Design and Implementation of a Bluetooth 4.0 LE Infrastructure for Mobile Devices", a thesis at ULM University.

[6] Sergio Aguilar, Rafael Vidal, and Carles Gomez, “Opportunistic Sensor Data Collection with Bluetooth Low Energy”, in Sensors 2017, 17(1).

[7] Bluetooth 5 Specifications published by Bluetooth SIG.

[8] ABI Research “Bluetooth Smart Evolution Helps the Technology Break into Key IoT Market Verticals” in PRNewswire, London, Nov-2016.

[9] Dixys L. Hernández-Rojas, Tiago M. Fernández-Caramés, Paula Fraga-Lamas, and Carlos J. Escudero, "Design and Practical Evaluation of a Family of Lightweight Protocols for Heterogeneous Sensing through BLE Beacons in IoT Telemetry Applications" in Sensors, 18(1), 57(2018).

[10] Kang Eun Jeon, James She, Perm Soonsawad, and Pai Chet Ng, "BLE Beacons for the Internet of Things Applications: Survey, Challenges, and Opportunities" in IEEE IoT Journal, 2018.

[11] Feng Yin, Yuxin Zhao, Fredrik Gunnarsson, and Fredrik Gustafsson, "Received-Signal-Strength threshold optimization using Gaussian processes," in IEEE Transaction on Signal Processing, vol. 65(8), April-2017.

[12] Neal Patwari and Alfred O. Hero III, "Using proximity and quantized RSS for sensor localization in wireless networks," in WSNA’03, San Diego, California, USA, September-2003.

[13] Xiaolong Shen, Shengqi Yang, Jian He, and Zhangqin Huang, "Improved localization algorithm based on RSSI in low power Bluetooth network" in IEEE 2016 2nd International Conference on Cloud Computing and Internet of Things (CCIOT), October-2016.

[14] Adel Thaljaoui, Thierry Val, Nejah Nasri, and Damien Brulin, "BLE localization using RSSI measurements and iRingLA," in IEEE International Conference on Industrial Technology (ICIT-2015), Spain, March-2015.

[15] Alasdair Allan and Sandeep Mistry, “Hacking the CES scavenger hunt”.

[16] Alasdair Allan and Sandeep Mistry, “Hacking the CES scavenger hunt for a second time”, October-2019.

[17] Prasant Misra, Shahid Raza, Vasanth Rajaraman, Jay Warrior, and Thienmo Voigt, "Poster Abstract: Security challenges in indoor location sensing using Bluetooth LE broadcast," in Poster Demo Session 12th European Conference on wireless sensor networks, February-2015.

[18] Constantinos Kolias, Lucas Copi, Fengwei Zhang, and Angelos Stavrou, "Breaking BLE beacons for fun but mostly profit," in Proceeding, EuroSec’17, ACM 10th European Workshop on system security, USA, April-2017.

[19] Rajat Pugaliya, Jaydip Chabhadiya, Nirav Mistry, and Ankit Prajapati, "Smart Shopee using Beacon," in 2017 IEEE International Conference on STMCCCEM, Chennai, India, August-2017.

[20] Ivan Howitt, "Mutual interference between independent Bluetooth piconets", in IEEE Transactions on vehicular Technology, Vol. 52, No. 3, May-2003.

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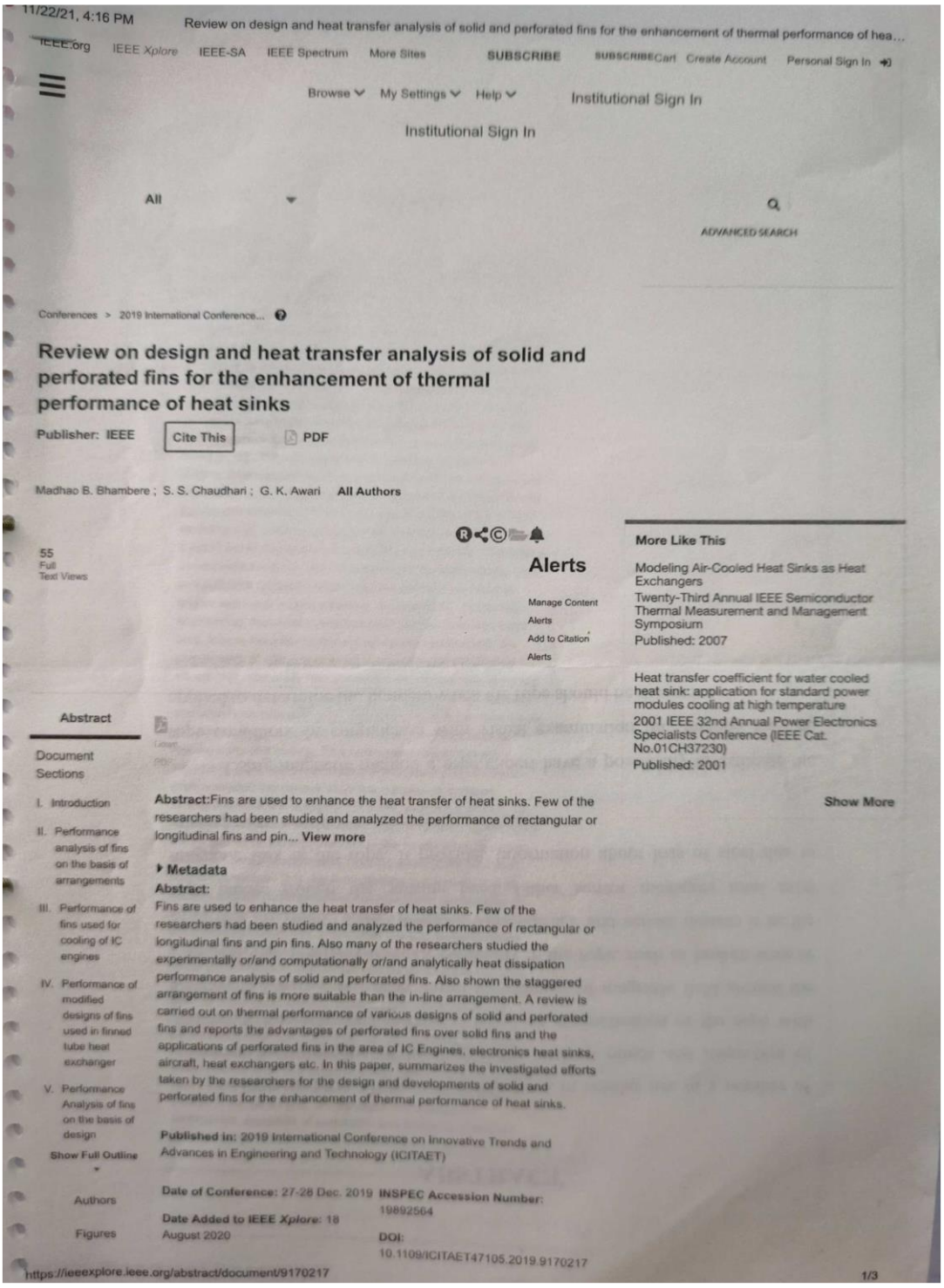

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Fins are used to enhance the heat transfer of heat sinks. Few of the researchers had been studied and analyzed the performance of rectangular or longitudinal fins and pin fins. Also many of the researchers studied the experimentally or/and computationally or/and analytically heat dissipation performance analysis of solid and perforated fins. Also shown the staggered arrangement of fins is more suitable than the in-line arrangement. A review is carried out on thermal performance of various designs of solid and perforated fins and reports the advantages of perforated fins over solid fins and the applications of perforated fins in the area of IC Engines, electronics heat sinks, aircraft, heat exchangers etc. In this paper, summarizes the investigated efforts taken by the researchers for the design and developments of solid and perforated fins for the enhancement of thermal performance of heat sinks.

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Determination of important parameters in lean Implementation in plastic pipe industries by Factor analysis

Dr. Javed.G Khan
Associate Professor, Dept of Mechanical Engineering
SSGM College of Engineering
Shegaon, India
itsjaweed@yahoo.co.in

Dr. Rajendra S Dalu
Professor, Dept of Mechanical Engineering
Government College of Engineering
Aurangabad, India
rsdalu@gmail.com

***Abstract*— Lean manufacturing is a people's driven activity hence people's factors play an important role in success of lean implementation. Most of the organizations are facing the challenges in the implementation of lean manufacturing. Majority of these challenges are organizational culture, commitment of the management, employees training and some technical issues. These challenges are main obstacle in the path of the lean implementation. To overcome such challenges, some important factors those play important role in the lean manufacturing process must be considered and their correlations must be examine critically. The main objective of this research paper is to critically examine the important factors affecting the success of lean Implementation in plastic pipe manufacturing industries.**

Keywords*— *Success factors, Lean manufacturing, Factor analysis

I. INTRODUCTION

Lean manufacturing is an approach in a systematic manner for identification as well as elimination of waste in various operations. To eliminate the waste, lean manufacturing focuses on continues improvement, reduction in operation cost, performing every process more efficiently and fulfilling the desire of the costumers by providing more values at the fewer prices [1]. The success of lean implementation is depends upon the correlation of the important parameters. To investigate the correlation between the important parameters factor analysis approach is selected in this research paper. Factor analysis is a multivariate statistical approach which is commonly use for real life applications. This tool is suitable when the numbers of independent variables are used for predicting a response variable. If the numbers of the independent variables in the data analysis are more, they increase the time for data collection and the computational time to get solutions. These can be avoided using factor analysis. Factor analysis focuses on grouping the original input variables into the factors which are underlie the input variables.

II. LITERATURE REVIEW

Many organizations face the challenges to apply lean. Most of these challenges are related to obstacles in the path of the lean implementation process such as executive, culture, management and technical issues. To successfully overcome these challenges, some critical factors must be considered in lean implementation process. From the comprehensive literature review on critical factors affecting the success of Lean implementation and survey of 42 plastic pipe industries of Vidarbha region of Maharashtra, the identified parameters in implementation of lean are as follows [1-6].

- Leadership and management of the organization
- Management commitment and Engagement in the implementation process.
- Willingness to do necessary changes in the organizational culture.
- Holistic approach by the management and employees
- Willingness to learn
- Employee Training
- Employee's involvement in all activities.
- Number of employees in the plant (skilled, semi skilled and unskilled)
- Awareness about lean manufacturing to the management and employees.
- Communication and Knowledge Sharing in the organization
- Suppliers Relationship
- Present manufacturing strategies in organization
- Size of the plant (small, medium or large)
- Production capacity of the plant (Yearly production)
- Different types of product produce by the plant.
- Financial capability of the organization
- Recognition of Financial benefits of lean
- Reward and compensation

III. METHODOLOGY FOR THE STUDY

To study the importance of different parameters of lean implementation a survey is carried out. In the survey, a structured questionnaire has been used as a data collection tool. Questionnaire has been divided into four parts: I) Leadership and management of the organization II) Skill and expertise in the organization III) Organizational culture and IV) Financial capability of the organization.

To understand the co-relation of the different factors, all the important factors are arrange in different groups. The table No.1 shows the arrangement of important parameters in different groups.

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Chapter 67
NO_x Reduction with Coherence of Particulate Matter for Single-Cylinder Diesel Engine Using Proportional EGR Technique

Chetan V. Bhusare and Kiran V. Chandan

Abstract Nowaday's oxides of nitrogen (NO_x) contribute major part in formation of pollutants in diesel engine. There are different types of emission reduction technologies are used to control the emissions but each technique has its merits and demerits. In current era, there is not a distinct technology existing to control NO_x exclusive of by-products. To optimize NO_x, various techniques are available which causes either energy consequence or raise other emissions terms of particulate matter. Proportional exhaust gas recirculation is one technique used to minimize NO_x in diesel engines. In present paper, NO_x is reduced by proportional EGR technique. The number of consistency trials was performed to achieve the required percentage of NO_x margin. But due to effect of EGR, it adversely affects the percentage value particulate matter; to overcome this problem, exhaust after treatment such as partial oxidation catalyst is used. With this proper hardware selection and experimental results, NO_x margin is improved by 10% and PM by 23%.

Keywords NO_x · Particulate matter · Proportional EGR · Partial oxidation catalyst

67.1 Introduction

The focus of present work is to optimize emissions using various latest technologies such as use of EGR for NO_x reduction and exhaust after treatment for CO, HC, and PM. Current baseline engine has passed the BS III emission norms. Due to customer's requirement, vehicles inertia is increased and this affects emissions which causes BS III failure. NO_x is the major concern after increasing the inertia.

Consequently, to meet up regulatory norms for emission, it is extremely desirous to reduce NO_x. In this paper, proportional EGR technique is used to reduce NO_x formation instead of continuous EGR. Using this technique, NO_x is reduced up to certain desired limit, but PM is increased randomly. Therefore, we have adopted exhaust

C. V. Bhusare (✉) · K. V. Chandan
Department of Mechanical Engineering, CSMSS CSCOE, Aurangabad, Maharashtra 431001, India
e-mail: chetanbhusare@gmail.com

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Comparative Analysis of Recent Neuro Fuzzy Systems For Stock Market Prediction

Pankaj K. Bharne ; Sameer S. Prabhune All Authors

Abstract:
The fuzzy logic and neural networks are the two powerful techniques commonly used in various application field from their evolution. The combination of both techniques is commonly termed as Neuro-Fuzzy System (NFS). Both techniques are combined because they overcome the limitations of each other. Basically, this model is used to construct the complex model by using fuzzy logic and its capabilities are improves with a neural network. In NFS, fuzzy rules are adjusted by the input-output patterns of a neural network. This paper presents the use of this powerful NFS system in the fields of stock market application for stock price prediction. Most of the traditional approaches do not consider all kind of stock price movements. But literature proves that the NFS is a leading technique in stock market prediction. This paper initially describes the brief description of neural networks and Fuzzy logic system along with their pros and cons. Further discussing, how the advantages of both systems combined in NFS. Also, the different types and architectures of NFS are presented here. Finally, this paper studies the recent NFS dependent methods which is used for the prediction of stock market. This paper summarizes the analysis of these techniques based on the technique used, the dataset used, their advantages and some research gap of all these techniques.

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